Buck Converter Design Issues

Master thesis performed in *division of Electronic Devices*
by

Muhammad Saad Rahman

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at

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Abstract

Switch Mode Power Supplies are very important components in present day electronics and have continued to thrive and grow over the past 25 years. This thesis looks inside how the SMPS have evolved over the passage of years with special emphasis to the Synchronous Buck Converter. It also discusses why there is a strong potential to further the study related to designs based around a Synchronous Buck Converter for portable applications. The main objective of the thesis is to look into the controller design for minimizing size, enhancing efficiency and reliability of power converters in portable electronic equipment such as mobile phones and PDAs. The thesis aims to achieve this using a 90 nm process with an input voltage of 1.55V and an output of 1V with a power dissipation of 200 mW.

Key Words: Switch Mode Power Supplies, Buck Converter, Voltage Mode Control, Compensator

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Abbreviations

BJT	Bipolar Junction Transistor
CCM	Continuous Conduction Mode
CMC	Current Mode Control
CMOS	Complementary MOS
DC	Direct Current
DCM	Discontinuous Conduction Mode
DCR	Direct Current Resistance
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NFET	Negative Channel Field Effect Transistor
PDA	Personal Digital Assistants
PFM	Pulse Frequency Modulation
PWM	Pulse Width Modulation
SMPS	Switch Mode Power Supplies
SRBC	Synchronous Rectifier Buck Converter
VLSI	Very Large Scale Integration
VMC	Voltage Mode Control

Abstract

Switch Mode Power Supplies (SMPS) are very important components in present day electronics and have continued to thrive and grow over the past 25 years. This thesis looks inside how the SMPS have evolved with special emphasis to the Synchronous Rectifier Buck Converter (SRBC). It also discusses why there is a strong potential to further the study related to designs based around a SRBC for portable applications. The main objective of the thesis is to look into the controller design for minimizing size, enhancing efficiency and reliability of power converters in portable electronic equipment such as mobile phones and PDAs. The thesis aims to achieve this using a 90nm process with an input voltage of 1.55V and an output of 1V with a power dissipation of approximately 200mW.

Preface

This master thesis is related to the design of a Buck Converter. Prof. Dr. Atila Alvandpour is the thesis examiner/supervisor and Lic. Henrik Fredriksson is the co-supervisor of my thesis work. Master thesis consists of 20 Swedish point's equivalent to 30 ECTS points.

The scope of thesis work includes the study of a Buck Converter and the issues involved in designing a Buck Converter. How a Buck Converter works with different types of isolation, the different kinds of modes available in Buck Converter, the Mode for which it has to be designed (Current Control / Voltage Mode), the design of the controller and the most important part of the designing of the Compensator. The system level study has been conducted using MATLAB and then simulated using the 90nm library.

Chapter 1 introduces the issues involved in power supplies. It also looks at why SMPS are preferred and concludes with a comparison between the Linear and Switch Mode Regulators.

Chapter 2 describes what SMPS are and what their current applications are. Also it briefly explains the different type of converters available.

Chapter 3 throws light on the actual Buck Converter and the theory of operation of the Buck Converter. The topics covered are how we reach to the SRBC which is used in this thesis. It also discusses the different mode – Continuous and the Discontinuous mode.

Chapter 4 deals with the Control of the Buck Converter. It discusses the PWM and the different techniques used in the control such as the Voltage Mode Control and the Current Mode Control.

Chapter 5 deals with the step by step designing of the Buck Converter and its subsequent controller based on the requirements of a 1.55V input and a 1 V output with 200mW output power. The chapter proceeds in a step by step manner in designing a Buck Converter.

Chapter 6 covers all the references that have been consulted for the preparation of this thesis report.

Dedicated to Mummy and Abbi, who have always supported me in all my endeavours …..

Acknowledgments

First of all I am thankful to Almighty Allah who has provided me the strength to successfully complete my Masters Thesis. Though their have been so many people who have played a role for my successful completion of my Masters Degree but to mention a few who have played a very major role:

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Muhammad Asif & Asad Ali the "Company" which was very understanding towards the final stages of my thesis work and also all the other residents of 12A: Ghassan Bhatti, Muhammad Tanveer, Waqar-ul-Hasan & Taimur Shahzad.

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1. Introduction

Over the years as the portable electronics industry progressed, different requirements evolved such as increased battery lifetime, small and cheap systems, brighter, full-colour displays and a demand for increased talk-time in cellular phones. An ever increasing demand from power systems has placed power consumption at a premium. To keep up with these demands engineers have worked towards developing efficient conversion techniques and also has resulted in the subsequent formal growth of an interdisciplinary field of Power Electronics. However it comes as no surprise that this new field has offered challenges owing to the unique combination of three major disciplines of electrical engineering: electronics, power and control [3].

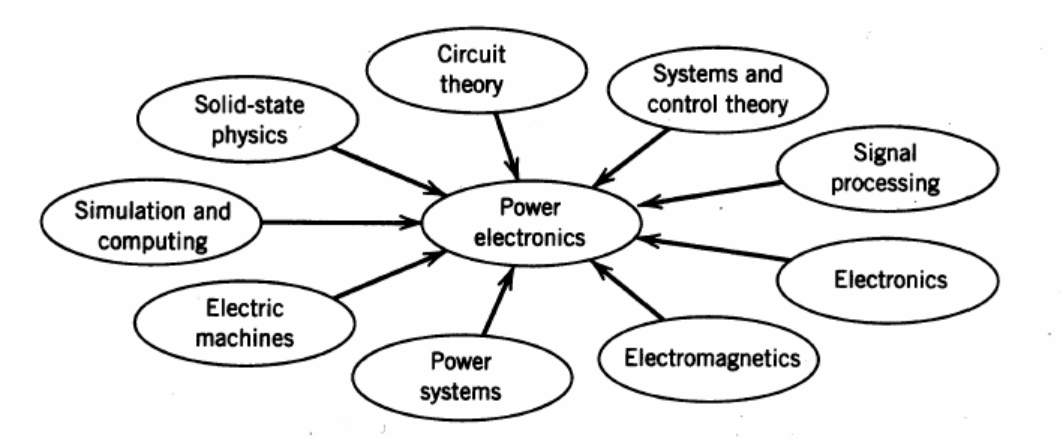

Figure 1: Interdisciplinary nature of Power Electronics [1]

These multi-discipline technologies, as highlighted in Figure 1-1, have involved control theory, filter synthesis, signal processing, thermal control, and magnetic components design [8].

This thesis looks at the design issues associated with designing dc/dc converters (Figure 1-2).

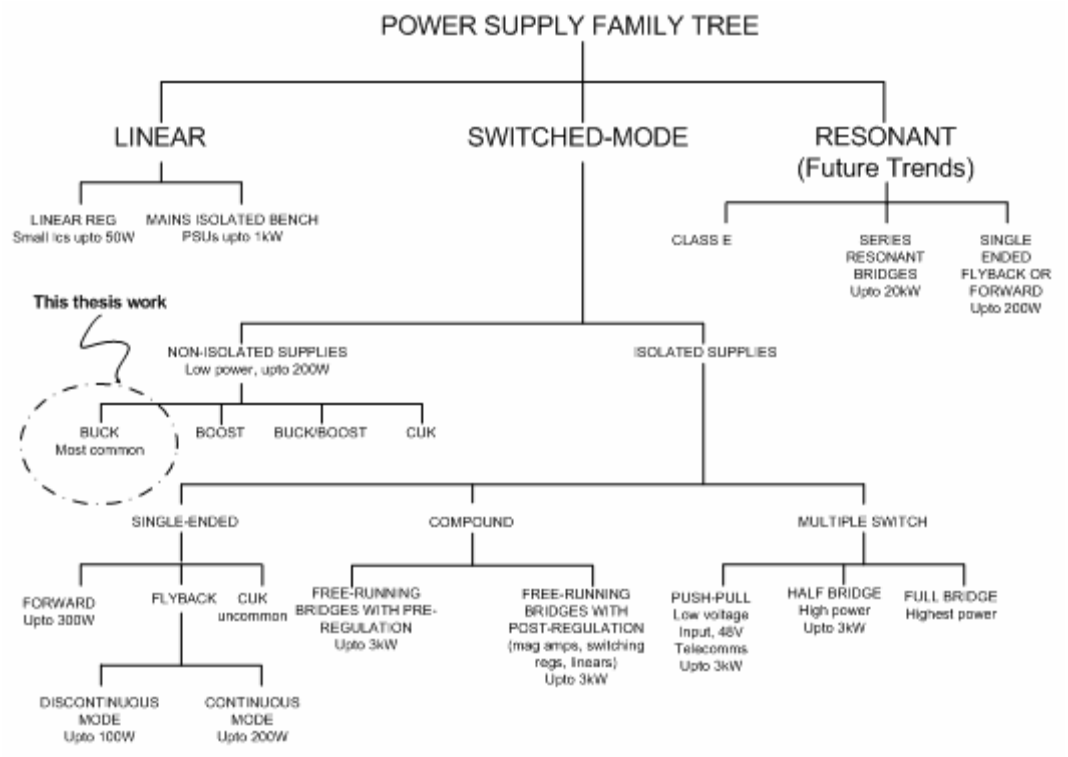

Figure 2: Power Supply Tree [27]

1.2 Why use a switching regulator?

Voltage regulation conventionally has been done by Linear Regulators but slowly is being replaced with Switching Regulators. To realize the importance of a switching regulator we will first compare its efficiency with a linear regulator. The resistance of the linear regulator varies in accordance with the load resulting in a constant output voltage [16].

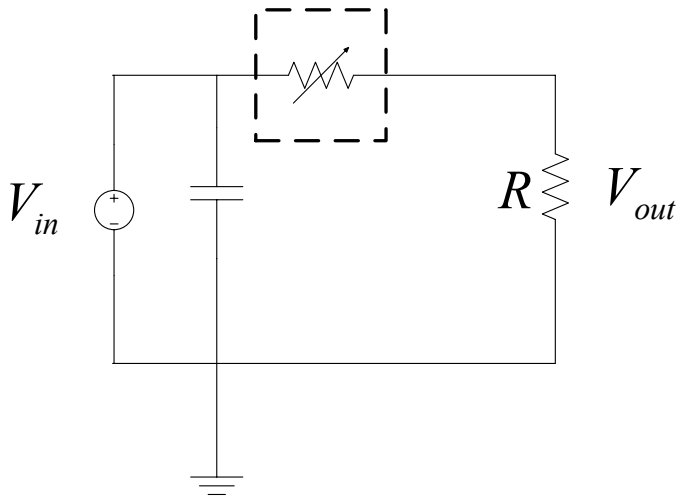

Figure 3: Linear Regulator

Figure 1-3 shows a simple Linear Regulator. If we consider an example, where V_{in} = 24 and we want to have a V_{out} = 12. In this case we need to drop 12 volts across the regulator.

Using standard power equation:

$$P = I \cdot V \qquad \text{(Eq. 1-1)}$$

If the output current = 10A, this will result in 10 A * 12 V = 120 W.

Now the regulator must dissipate 120 W of heat energy. This results in a mere 50% efficiency for the linear regulator and a lot of wasted power which is normally transformed into heat. Provision for heat sinks for cooling makes the regulator bulky and large. Hence, where size and efficiency are critical, linear voltage regulators cannot be used.

Figure 1-4 is a very basic switching regulator. The switching regulator is a simple switch (and hence ideally no resistance or very low resistance). This switch goes on and off at a fixed rate (usually between 50 KHz to 100 KHz) as shown in Figure 1-4.

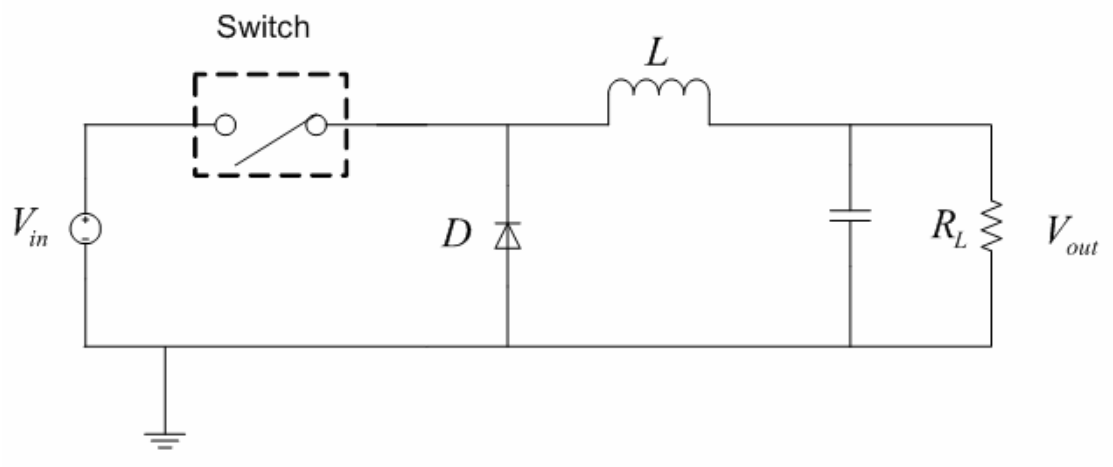

Figure 4: Switching Regulator

The Duty Cycle for the switch is determined by the Eq. 1-2.

$$Duty \quad Cycle = \frac{V_{out}}{V_{in}} \qquad \text{(Eq. 1-2)}$$

The time that the switch remains closed during each switch cycle is varied to maintain a constant output voltage. The switching regulator is much more efficient than the linear regulator achieving efficiencies as high as 80% to 95% in some circuits. In contrast, the linear regulator usually exhibits only 50% to 60% efficiency. With higher efficiency smaller heat sinks will be required because lesser heat is dissipated. This further results in SMPS, that can be packaged in a fraction of the size of linear regulators.

There is also another advantage of Switching Regulators and that is that the energy stored by inductor & capacitor can be transformed to output voltages that can be greater than input (boost), negative (inverter), or can be transferred through a transformer to provide electrical isolation with respect to the input.

Unlike linear regulators, switched power supplies can step up or step down the input voltage [14].

All of our discussion can be summarized with a comparison in Table 1:

	Linear	Switching
Function	**Only steps down**; input voltage must be greater than output.	**Steps up, steps down, or inverts**
Efficiency	**Low to medium,** but actual battery life depends on load current and battery voltage over time; **high** if V_{IN}-V_{OUT} difference is small.	**High,** except at very low load currents (μA), where switch-mode quiescent current is usually higher.
Waste Heat	**High,** if average load and/or input/output voltage difference are high	**Low,** as components usually run cool for power levels below 10W
Complexity	**Low,** which usually requires only the regulator and low-value bypass capacitors	**Medium to high,** which usually requires inductor, diode, and filter caps in addition to the IC; for high-power circuits, external FETs are needed
Size	**Small to medium** in portable designs, but may be larger if heat sinking is needed	Larger than linear at low power, but smaller at power levels for which linear requires a heat sink
Total Cost	**Low**	**Medium to high,** largely due to external components
Ripple/Noise	**Low**; no ripple, low noise, better noise rejection.	**Medium to high,** due to ripple at switching rate

Table 1: Comparison between Linear and Switch-Mode Regulators [17]

2. DC-DC Converter

2.1 Introduction

DC-DC converters are electronic devices that are used whenever we want to change DC electrical power efficiently from one voltage level to another. In the previous chapter we mentioned the drawbacks of doing this with a linear regulator and presented the case for SMPS. Generically speaking the use of a switch or switches for the purpose of power conversion can be regarded as a SMPS. From now onwards when ever we mention DC-DC Converters we shall address them with respect to SMPS.

A few applications of interest of DC-DC converters are where 5V DC on a personal computer motherboard must be stepped down to 3V, 2V or less for one of the latest CPU chips; where 1.5V from a single cell must be stepped up to 5V or more, to operate electronic circuitry. In all of these applications, we want to change the DC energy from one voltage level to another, while wasting as little as possible in the process. In other words, we want to perform the conversion with the highest possible efficiency.

DC-DC Converters are needed because unlike AC, DC can't simply be stepped up or down using a transformer. In many ways, a DC-DC converter is the DC equivalent of a transformer. They essentially just change the input energy into a different impedance level. So whatever the output voltage level, the output power all comes from the input; there's no energy manufactured inside the converter. Quite the contrary, in fact some is inevitably used up by the converter circuitry and components, in doing their job.

2.2 What are SMPS?

High frequency switching converters are power circuits in which the semiconductor devices switch at a rate that is *fast compared to the variation of the input and output waveforms*. Figure 2-1 shows a generic block diagram of a SMPS. The difference between the switching frequency and the frequency of the external waveforms is large enough to permit the use of low-pass filters to remove the unwanted switching frequency components. High frequency switching converters are used most often as interfaces between dc systems of different voltage levels. These converters are known as *high-frequency dc/dc converters*, and examples of their use are the power supplies in computers and other electronic equipment. High frequency switching converters can also be

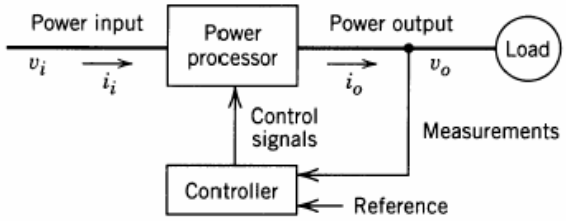

Figure 5: Block Diagram of a Switch Mode Power Supply [1]

used as an interface between dc and ac systems [18].

2.3 Types of Converters

Currently, dc/dc converters can be divided into two broad categories:

- Non-isolated dc/dc converters
- Isolated dc/dc converters

2.3.1 Non-Isolated DC/DC Converters

The non-isolated converter usually employs an inductor, and there is no dc voltage isolation between the input and the output. The vast majority of applications do not require dc isolation between input and output voltages. The non-isolated dc-dc converter has a dc path between its input and output.

Battery-based systems that don't use the ac power line represent a major application for non-isolated dc-dc converters. Point-of-load dc-dc converters that draw input power from an isolated dc-dc converter, such as a bus converter, represent another widely used non-isolated application.

Most of these dc-dc converter ICs use either an internal or external synchronous rectifier. Their only magnetic component is usually an output inductor and thus less susceptible to generating electromagnetic interference. For the same power and voltage levels, it usually has lower cost and fewer components while requiring less pc-board area than an isolated dc-dc converter. For lower voltages (12V) non-isolated buck converters can be used.

2.3.2 Isolated DC/DC Converters

For safety considerations, there must be isolation between an electronic system's ac input and dc output. Isolation requirements cover all systems operating from the ac power line, which can include an isolated front-end ac-dc power supply

followed by an isolated "brick" dc-dc converter, followed by a non-isolated point-of-load converter. Typical isolation voltages for ac-dc and dc-dc power supplies run from 1500 to 4000V, depending on the application. An isolated converter employs a transformer to provide dc isolation between the input and output voltage which eliminates the dc path between the two.

Isolated dc-dc converters use a switching transformer whose secondary is either diode-or synchronous-rectified to produce a dc output voltage using an inductor-capacitor output filter. This configuration has the advantage of producing multiple output voltages by adding secondary transformer windings. For higher input voltages (48V) transformer isolated converters are more viable [19].

2.4 Why work on Buck Converters?

The buck converter is the most widely used dc-dc converter topology in power management and microprocessor voltage-regulator (VRM) applications. Those applications require fast load and line transient responses and high efficiency over a wide load current range. They can convert a voltage source into a lower regulated voltage. For example, within a computer system, voltage needs to be stepped down and a lower voltage needs to be maintained. For this purpose the Buck Converter can be used [20]. Furthermore buck converters provide longer battery life for mobile systems that spend most of their time in "stand-by". Buck regulators are often used as switch-mode power supplies for baseband digital core and the RF power amplifier (PA) [35].

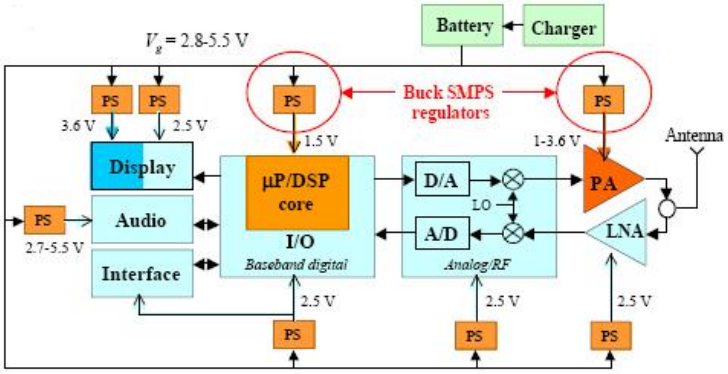

Figure 6: Buck regulators in the system [35]

3. Buck Converter – Theory of Operation

The name "Buck Converter" presumably evolves from the fact that the input voltage is bucked/chopped or attenuated, in amplitude and a lower amplitude voltage appears at the output. A buck converter, or step-down voltage regulator, provides non-isolated, switch-mode dc-dc conversion with the advantages of simplicity and low cost. Figure 7 shows a simplified non-isolated buck converter that accepts a dc input and uses pulse-width modulation (PWM) of switching frequency to control the output of an internal power MOSFET. An external diode, together with external inductor and output capacitor, produces the regulated dc output.

Buck, or step down converters produce an average output voltage lower than the input source voltage.

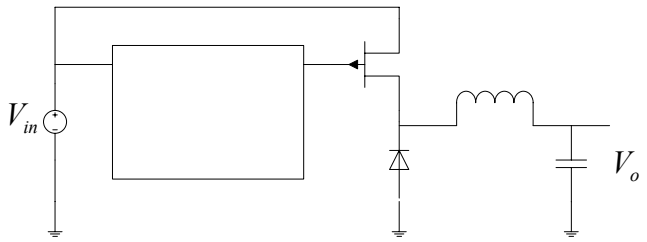

Figure 7: Complete Switching Regulator Topology

3.1 Evolution of a Buck Converter

The buck converter here onwards is introduced using the evolutionary approach. Let us consider the circuit in Figure 8, containing a single pole double-throw switch.

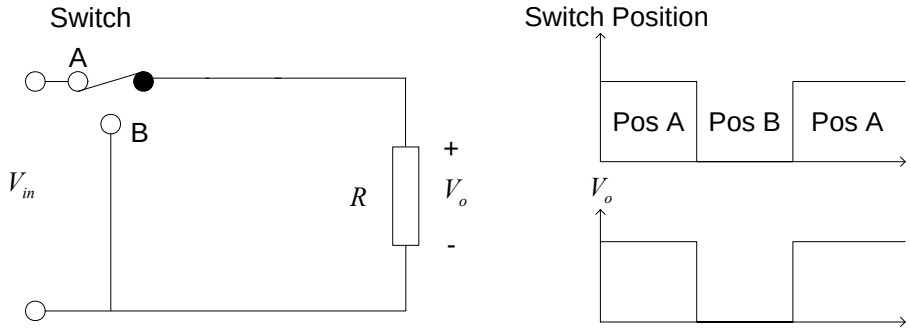

Figure 8: A resistor with a single-pole double-throw switch

For the circuit in Figure 8, the output voltage equals the input voltage when the switch is in position A and it is zero when the switch is in position B. By varying the duration for which the switch is in position A and B, it can be seen that the average output voltage can be varied, but the output voltage is not pure dc. The circuit in Figure 8 can be modified as shown in Figure 9 by adding an inductor in series with the load resistor. An inductor reduces ripple in current passing through it and the output voltage would contain less ripple content since the current through the load resistor is the same as that of the inductor. When the switch is in position A, the current through the inductor increases and the energy stored in the inductor increases. When the switch is in position B, the inductor acts as a source and maintains the current through the load resistor. During this period, the energy stored in the inductor decreases and its current falls. It is important to note that there is continuous conduction through the load for this circuit. If the time constant due to the inductor and load resistor is relatively large compared with the period for which the switch is in position A or B, then the rise and fall of current through inductor is more or less linear, as shown in Figure 9.

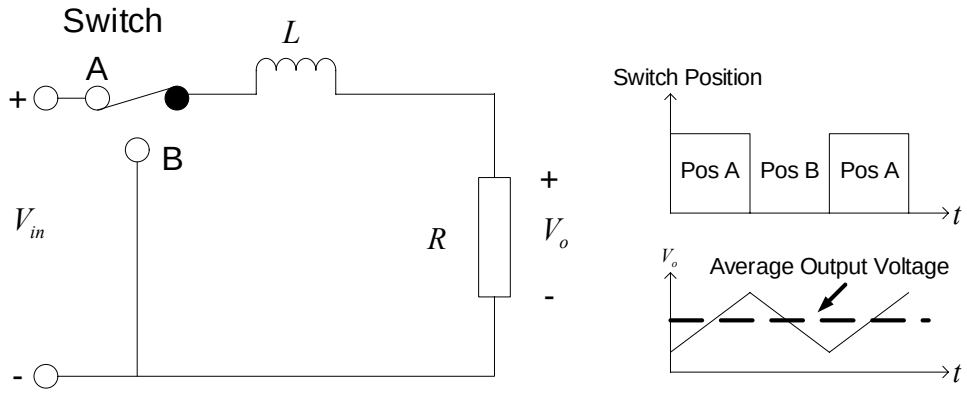

Figure 9: Effect of an Inductor

The next step in the evolutionary development of the buck converter is to add a capacitor across the load resistor and this circuit is shown in Figure 10. A capacitor reduces the ripple content in voltage across it, whereas an inductor smoothes the current passing through it. The combined action of LC filter reduces the ripple in output to a very low level.

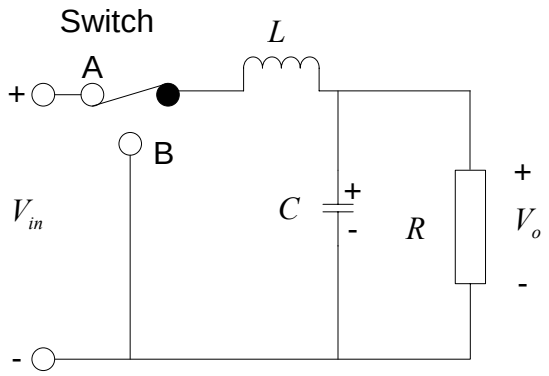

Figure 10: Circuit with an LC Filter

With the circuit in Figure 10 it is possible to have a power semiconductor switch to correspond to the switch in position A and a diode in position B. The circuit that results is shown in Figure 11. When the switch is in position B, the current will pass through the diode. The important thing now is the controlling of the power semiconductor switch.

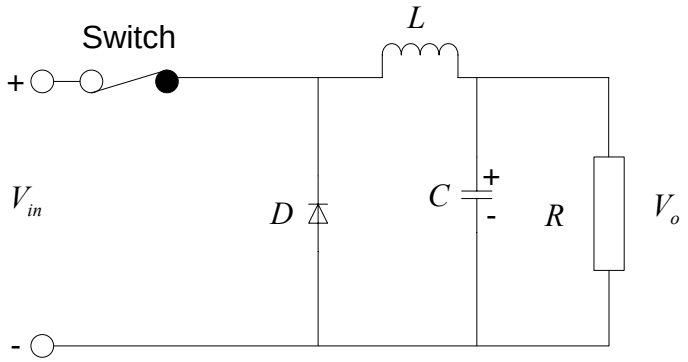

Figure 11: Buck Converter with load resistor

The circuit in Figure 11 can be regarded as the most elementary buck converter without a feedback. The Buck Converter transfers small packets of energy with the help of a power switch, a diode, and an inductor and is accompanied by an output filter capacitor and input filter. All the other topologies such as the Boost, Buck-Boost Converter etc, vary by the different arrangement of these basic components.

This circuit can be further modified by adding the feedback part which is integral for a SMPS because based on the feedback it stabilizes the output. Such a circuit is shown in the Figure 12.

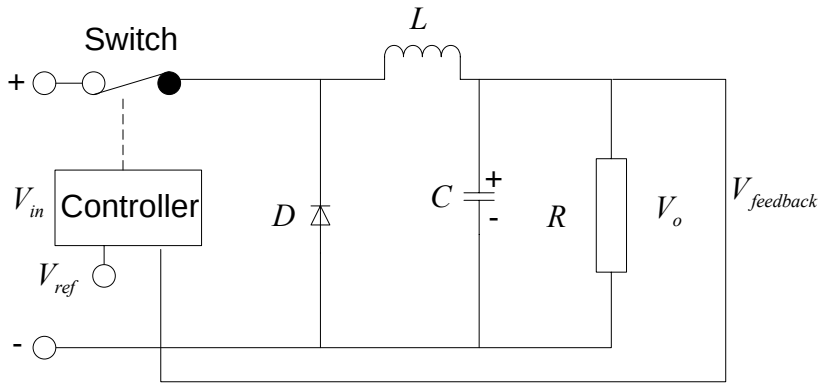

Figure 12: Step Down Switch Mode Power Supply

The PWM Controller (Figure 12) compares a portion of the rectified dc output with a voltage reference (V_{ref}) and varies the PWM duty cycle to maintain a constant dc output voltage. If the output voltage wants to increase, the PWM lowers its duty cycle to reduce the regulated output, keeping it at its proper voltage level. Conversely, if the output voltage tends to go down, the feedback causes the PWM duty cycle to increase and maintain the proper output. A buck converter or step-down switch mode power supply can also be called a switch mode regulator [21].

3.2 Purpose of different components in the Buck Converter

As just seen in the previous section that any basic switched power supply consists of five standard components:

- pulse-width modulating controller
- transistor switch (active switch)
- inductor
- capacitor
- diode (passive switch)

Now we will look into more detail as to the selection and the functioning of these components.

3.2.1 Switch

In its crudest form a switch can be a toggle switch which switches between supply voltage and ground. But for all practical applications which we shall consider we will deal with transistors. Transistors chosen for use in switching

power supplies must have fast switching times and should be able to withstand the voltage spikes produced by the inductor. The input on the gate of the transistor is normally a Pulse Width Modulated (PWM) signal which will determine the ON and OFF time. Sizing of the power switch is determined by the load current and off-state voltage capability.

The power switch (transistor) can either be a MOSFET, IGBT, JFET or a BJT. Power MOSFETs are the key elements of high frequency power systems such as high-density power Supplies [2]**.** Therefore MOSFETs have now replaced BTJ's in new designs operating at much higher frequencies but at lower voltages. At high voltages MOSFETs still have their limitations. The intrinsic characteristics of the MOSFET produce a large on-resistance which increases excessively when the devices' breakdown voltage is raised. Therefore, the power MOSFET is only useful up to voltage ratings of 500V and so is restricted to low voltage applications or in two-transistor forward converters and bridge circuits operating off-line. At high breakdown voltages (>200V) the on-state voltage drop of the power MOSFET becomes higher than that of a similar size bipolar device with similar voltage rating. This makes it more attractive to use the bipolar power transistor at the expense of worse high frequency performance [28]. As improvements in fabrication techniques, new materials, device characteristics take place than MOSFETs are likely to replace BJTs.

Another new device likely to displace the BJT in many high power applications is the Insulated Gate Bipolar Transistor (IGBT). This device combines the low power drive characteristics of the MOSFET with the low conduction losses and high blocking voltage characteristics of the BJT. Therefore the device is highly suited to high power, high voltage applications. However, since current transport in the
device is by the same process as the BJT, its switching speed is much slower than the MOSFET, so the IGBT is at present limited to lower (<50kHz) applications [31].

Operating Frequency

The operating frequency determines the performance of the switch. Switching frequency selection is typically determined by efficiency requirements. There is now a growing trend in research work and new power supply designs in increasing the switching frequencies. The higher is the switching frequency, the smaller the physical size and component value. The reason for this is to reduce even further the overall size of the power supply in line with miniaturisation trends in electronic and computer systems.

However, there is an upper frequency limit where either magnetic losses in the inductor or switching losses in the regulator circuit and power MOSFET reduce efficiency to an impractical level. Higher frequency also reduces the size of the output capacitor. E.g., the capacitance required is 67µF at 500 KHz, but only 33µF at 1MHz. The ripple current specification remains unchanged [24].

3.2.2 Inductor

The function of the inductor is to limit the current slew rate (limit the current in rush) through the power switch when the circuit is ON. The current through the inductor cannot change suddenly. When the current through an inductor tends to fall, the inductor tends to maintain the current by acting as a source. This limits the otherwise high-peak current that would be limited by the switch resistance alone. The key advantage is when the inductor is used to drop voltage, it stores energy. Also the inductor controls the percent of the ripple and determines whether or not the circuit is operating in the continuous mode.

Peak current through the inductor determines the inductor's required saturation-current rating, which in turn dictates the approximate size of the inductor. Saturating the inductor core decreases the converter efficiency, while increasing the temperatures of the inductor, the MOSFET and the diode. The size of the inductor and capacitor can be reduced by the implementation of high switching frequency, multi-phase interleaved topology, and a fast hysteric controller [30].

A smaller inductor value enables a faster transient response; it also results in larger current ripple, which causes higher conduction losses in the switches, inductor, and parasitic resistances. The smaller inductor also requires a larger filter capacitor to decrease the output voltage ripple.

Inductors used in switched supplies are some times wound on toroidal cores, often made of ferrite or powdered iron core with distributed air-gap to store energy.

A DC-DC converter transfers energy at a controlled rate from an input source to an output load, and as the switching frequency increases, the time available for this energy transfer decreases. For example, consider a buck converter operating at 500 kHz with a 10 µH inductor. For most DC-DC converters, changing the frequency to 1 MHz allows use of exactly one half the inductance, or 5µH.

3.2.3 Capacitor

Capacitor provides the filtering action by providing a path for the harmonic currents away from the load. Output capacitance (across the load) is required to minimize the voltage overshoot and ripple present at the output of a step-down converter. The capacitor is large enough so that its voltage does not have any noticeable change during the time the switch is off. Large overshoots are caused by insufficient output capacitance, and large voltage ripple is caused by insufficient capacitance as well as a high equivalent-series resistance (ESR) in the output capacitor. The maximum allowed output-voltage overshoot and ripple are usually specified at the time of design. Thus, to meet the ripple specification for a step-down converter circuit, we must include an output capacitor with ample capacitance and low ESR.

The problem of overshoot, in which the output-voltage overshoots its regulated value when a full load is suddenly removed from the output, requires that the output capacitor be large enough to prevent stored inductor energy from launching the output above the specified maximum output voltage.

Since switched power regulators are usually used in high current, high-performance power supplies, the capacitor should be chosen for minimum loss. Loss in a capacitor occurs because of its internal series resistance and inductance. Capacitors for switched regulators are partly chosen on the basis of Effective Series Resistance (ESR). Solid tantalum capacitors are the best in this respect [9]. For very high performance power supplies, sometimes it is necessary to parallel capacitors to get a low enough effective series resistance.

3.2.4 Freewheeling Diode/Transistor

Since the current in the inductor cannot change suddenly, a path must exist for the inductor current when the switch is off (open). This path is provided by the freewheeling diode (or catch diode).

The purpose of this diode is not to rectify, but to direct current flow in the circuit and to ensure that there is always a path for the current to flow into the inductor. It is also necessary that this diode should be able to turn off relatively fast. Thus the diode enables the converter to convert stored energy in the inductor to the load. This is a reason why we have higher efficiency in a DC-DC Converter as compared to a linear regulator. When the switch closes, the current rises linearly (exponentially if resistance is also present). When the switch opens, the freewheeling diode causes a linear decrease in current. At steady state we have a saw tooth response with an average value of the current.

In many circuits and the one we will be discussing such as the Synchronous Buck Converter we will see that the Freewheeling diode is replaced by the Negative Field Effect Transistor (NFET). The reasons for this in short are to increase the efficiency. The 0.7 V forward voltage drop (or a little less with a Schottky diode) is a main source of efficiency loss in the buck regulator at low voltages. An alternative is to use a transistor in saturation (0.2V or 0.3V) to provide the flywheel function. This arrangement does raise some complications because the buck regulator has to synchronously turn on the flywheel element at just the right times, in order to keep the current flowing smoothly. The diode solution turns itself on and off, so it does not require a synchronous flywheel drive signal. The active circuit with the synchronous flywheel transistor is generally more expensive than the simple passive diode circuit, but the gain in efficiency (P_{out}/P_{in}) is sometimes worth the extra cost. But in any case we have a Schottky in parallel with the flywheel transistor, rather than a Zener. A well saturated transistor will have a lower V_{ds} than the Schottky diode, but the diode will help ease/guarantee the switching transition.

3.2.5 Feedback

Feedback and control circuitry can be carefully nested around these circuits to regulate the energy transfer and maintain a constant output within normal operating conditions. Control by pulse-width modulation is necessary for regulating the output. The transistor switch is the heart of the switched supply and it controls the power supplied to the load. More of this will be discussed in Chapter 4.

3.3 States of Operation

There are two states in which the circuit given in Figure 13 operates. That is the ON State and the OFF State. These two states and the active circuit part for those given states are shown in the Figure 14 & Figure 15.

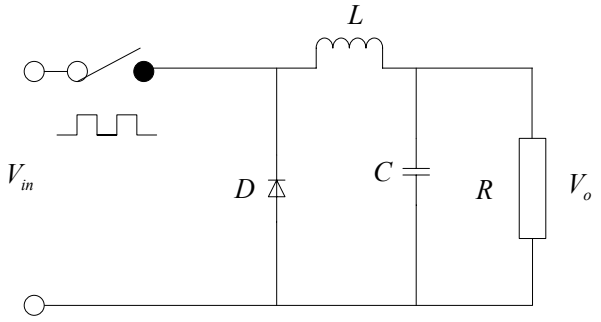

Figure 13: General Buck Converter Schematic

3.3.1 ON State

The operation of the buck converter is fairly simple, with an inductor and two switches (usually a transistor and a diode) that control the inductor. It alternates between connecting the inductor to source voltage to store energy in the inductor and discharging the inductor into the load.

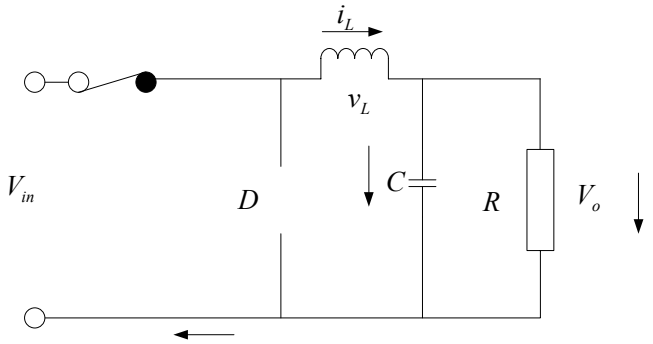

Figure 14: ON State

Refer to Figure 14, when the switch is connected, L is connected to the switch which tends to oppose the rising current and begins to generate an electromagnetic field in its core. Diode D is reverse biased and is essentially an open circuit at this point. The inductor current increases, inducing a positive voltage drop across the inductor and a lower output supply voltage in reference to the input source voltage. The inductor serves as a current source to the output load impedance.

3.3.2 OFF State

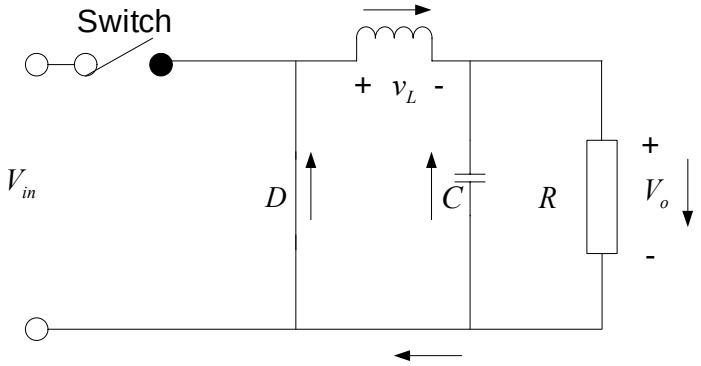

Figure 15: OFF State

In the OFF state the switch is open, diode D conducts and energy is supplied from the magnetic field of L and electric field of C. The current through the inductor falls linearly. When the FET switch is off, the inductor current discharges, inducing a negative voltage drop across the inductor. Because one port of the inductor is tied to ground, the other port will have a higher voltage level, which is the target output supply voltage. The output capacitance acts as a low-pass filter, reducing output voltage ripple as a result of the fluctuating current through the inductor. The diode prevents the current flowing from the inductor when the FET switch is off.

3.3.3 Continuous Mode / Discontinuous Mode

During the ON state and than the subsequent OFF state the Buck Converter can operate in Continuous Mode or Discontinuous Mode. The difference between the two is that in CCM the current in the inductor does not fall to zero. See Figure 16

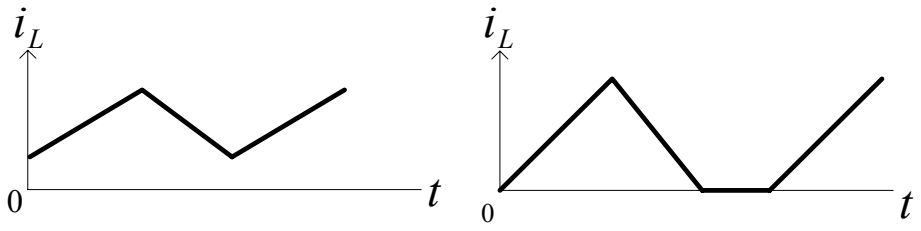

Figure 16: (a) Continuous Mode (b) Discontinuous Mode

Current flows continuously in the inductor during the entire switching cycle in steady state operation. In most Buck regulator applications, the inductor current never drops to zero during full-load operation. Overall performance is usually better using continuous mode, and it allows maximum output power to be obtained from a given input voltage and switch current rating. Energy from the battery is supplying the load and is being stored in the inductor L as a magnetic field. The current through the inductor is rising linearly.

In the DCM the current in the inductor falls to zero and remains at zero for some portion of the switching cycle. It starts at zero, reaches a peak value, and returns to zero during each switching cycle. In applications where the maximum load current is fairly low, it can be advantageous to design for discontinuous mode operation. In these cases, operating in discontinuous mode can result in a smaller overall converter size (because a smaller inductor can be used). Often the output capacitor must be large to keep the voltage constant.

3.4 Synchronous Buck Converters

3.4.1 Introduction

Synchronous buck converters have received great attention for low-voltage power conversion because of its high efficiency and reduced area consumption [4]. One of the main reasons for not using a synchronous FET earlier was that there was a much greater cost difference between FETs and Schottky diodes years ago. Moreover, since output voltages were generally higher (5V or greater), the drop across the Schottky was not as large a percentage as it is now. As FET technology has improved, providing better and better conductivity at ever lower price, the FET has become the main choice over the Schottky. Even more importantly, the "forward" voltage drop of the FET can be arbitrarily low compared to the Schottky a major issue with output voltages hovering around 1 volt. The synchronous buck topology is also considered suitable for Envelope Tracking Power Supply because of its simple dynamics and symmetrical slew-rate capability [6].

3.4.2 Topology

This topology uses the complementary switches (Figure 17) to transfer energy to the filter inductance from the power source.

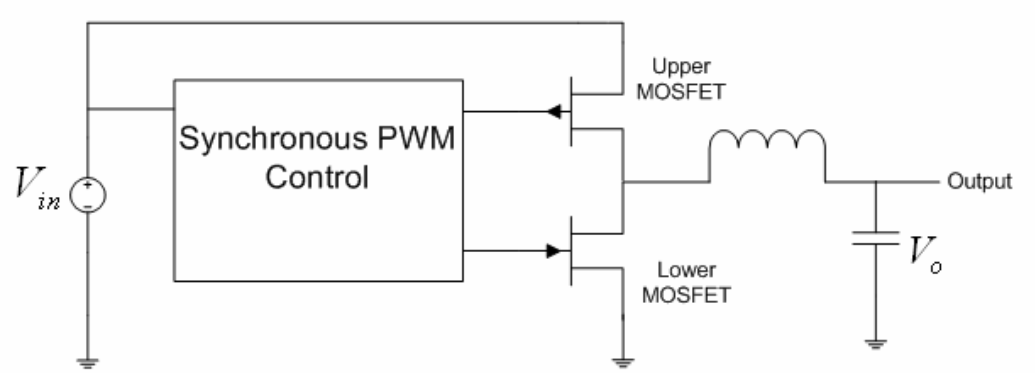

Figure 17: Complementary switches

The synchronous buck converter is essentially the same as the buck step-down converter with the substitution of the "catch" diode for another FET switch, or Synchronous Rectifier (SR). The upper MOSFET conducts to transfer energy from the input (same as the conventional buck converter) and charges the inductor current. When the switch control is off, the lower MOSFET switch turns on to circulate the inductor current and provides a current path for the inductor when discharging.

The control and driver circuits synchronize the timing of both MOSFETs with the switching frequency. The synchronous PWM control block regulates the output voltage by modulating the conduction intervals of the upper and lower MOSFETs. This topology improves efficiency with faster switch turn-on time and lower FET series resistance (r_{dson}) versus the diode. Under light loads, the control block usually turns the lower MOSFET off to emulate a diode[29], this is because more power is lost in turning a large FET switch on and off, than lost due to the resistance of the switch itself.

3.4.3 Improvements

Synchronous rectification increases the efficiency of a buck converter by replacing the Schottky diode with a low-side NMOS FET. The resultant voltage drop across the MOSFET can be smaller than the forward voltage drop of the Schottky diode. To show that the efficiency is greatly increased by replacing the diode with a MOSFET can be shown with the following set of equations. First consider the case when we have a diode. The equation for power loss across a diode can be calculated with Eq. 3-1.

$$P_D = V_D \cdot (1 - D) \cdot I_o \qquad \text{(Eq. 3-1)}$$

Note that it is multiplied with (1-D) for the OFF time. Because the diode conducts in the OFF state. Assume that the input is 5V and the output is 3.3 V, and the load current is 10A. In this case the duty cycle will be 66% and the diode will be ON for 34% of the time. A typical diode with a 0.7V would suffer a power loss of 2.38 W.

Now we take the equation for a switch

$$P_{S2} = I_o^2 \cdot R_{DSON} \cdot (1 - D) \qquad \text{(Eq. 3-2)}$$

It can be seen that the power loss is very much dependent upon the duty cycle. A synchronous rectifier generally has lower losses than a conventional or Schottky diode, and so its use is quite popular in low voltage DC/DC converters. Also for increased efficiency the following relation must be true $I_o^2 \cdot R_{DSON} << V_D$.

3.4.4 Problems

This topology requires more components and additional switch logic sequencing. Also this power conversion topology suffers from a degraded

efficiency at light loads [32] (because power is lost in turning on the device), a problem that can severely limit the battery lifetime of portable devices that spend a substantial amount of time in "stand-by" mode and hence resulting in a substantial reduction in converter efficiency. Since many portable devices operate in low-power standby modes for a majority of the time they are on, increasing light-load converter efficiency can significantly increase battery lifetime. The SRBC requires two off-chip passive filter components. These components greatly increase the overall size and cost of the system.

Synchronous rectification with discrete MOSFETs causes variable switching delays because of the variations in gate charge and threshold voltage from one MOSFET to another. Standard control circuits compensate for these variations by delaying the turn-on drive of the lower MOSFET until after the gate voltage of the upper MOSFET falls below a threshold. This delay creates a dead time in which neither MOSFET conducts. The dead time eliminates the possibility of a destructive shoot-through condition in which both MOSFETs conduct simultaneously. Standard designs use the same method to delay the turn-on of the upper device [29].

4. Practical Issues of Buck Converter

In the previous chapter we looked at the working of the Buck Converter. In this chapter we will derive the equations for practical calculations.

4.1 Calculation for Duty Ratio

For calculation of the duty ratio we will first of all assume that the converter is in steady state. (For steady state see Appendix C).The switches are treated as being ideal, and the losses in the inductive and the capacitive elements are neglected. Also it is important to point out that the following analysis does not include any parasitic resistances (all ideal case). The analysis also has the assumption that the converter is operating in Continuous conduction mode only i.e. $i_L(t) > 0$.

When the switch is on for time duration t_{on}, the switch conducts the inductor current and the diode becomes reverse biased. This results in a positive voltage $v_L = V_d - V_o$ across the inductor in Figure 18(a). This voltage causes a linear increase in the inductor current i_L. When the switch is turned off, because of the inductive energy storage, i_L continues to flow. This current now flows through the diode, and $v_L = -V_o$ in Figure 18 (b).

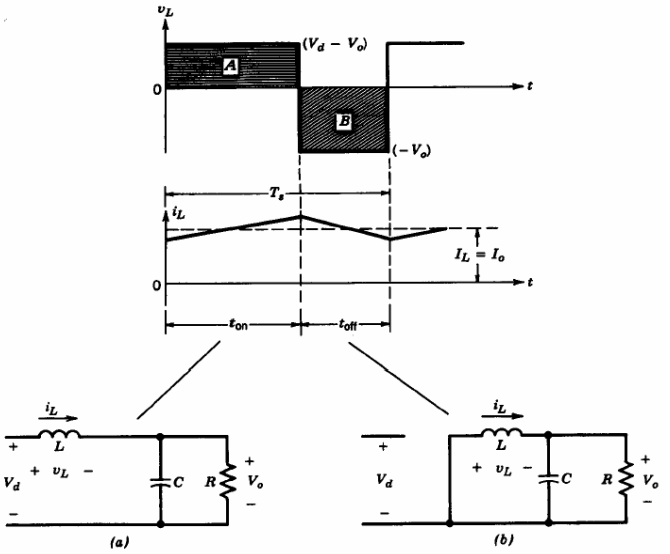

Figure 18: Step-down converter circuit states (assuming i_L flows continuously): (a) switch on; (b) switch off [1]

Since in steady-state operation waveform must repeat from one time period to the next, the integral of the inductor voltage v_L over one time period must be zero, where $T_s = t_{on} + t_{off}$:

$$\int_0^{T_s} v_L dt = \int_0^{t_{on}} v_L dt + \int_{t_{on}}^{T_s} v_L dt = 0 \qquad \text{(Eq. 4-1)}$$

From Figure 18, it implies that areas A and B must be equal (See Appendix C). Therefore,

$$(V_d - V_o)t_{on} = V_o(T_s - t_{on}) \qquad \text{(Eq. 4-2)}$$

or

$$\frac{V_o}{V_d} = \frac{t_{on}}{T_s} = D \text{ (duty ratio)} \qquad \text{(Eq. 4-3)}$$

Hence in this mode, the voltage output varies linearly with the duty ratio of the switch for a given input voltage and does not depend on any other circuit parameter.

4.2 Calculation for Inductor

From Figure 18(a) we can derive a simplified differential equation based on the assumption that the voltage across the load, and thereby across the capacitor, is fairly constant. The differential equation in terms of the current through the inductor, when the switch is closed, may now be written as

$$L\frac{di_L(t)}{dt} = V_d - V_o \qquad \text{(Eq. 4-4)}$$

Assuming that the circuit has assumed steady state hence there may already be some current in the inductor, $I_{L,\min}$, just prior to the closing of switch S. Hence for a time interval $0 \le t \le T_{ON} = DT$, gives:

$$i_L(t) = \frac{V_d - V_o}{L}t + I_{L,\min} \qquad \text{(Eq. 4-5)}$$

The inductor current increases linearly with time and attains its maximum value $I_{L,\max}$ as $t \to T_{ON} = DT$ such that

$$I_{L,\max} = \frac{V_d - V_o}{L} DT + I_{L,\min} \qquad \text{(Eq. 4-6)}$$

Defining the change in the current from its minimum to maximum value as the peak-to-peak current ripple ΔI_L, the equation 4-6 yields an expression for ΔI_L,as

$$\Delta I_L = I_{L,\max} - I_{L,\min} = \frac{V_d - V_o}{L} DT \qquad \text{(Eq. 4-7)}$$

Note that the current ripple is directly proportional to D, the duty cycle, upon which we may not have any control because of the output voltage requirement. However, it is inversely proportional to the inductance L upon which we can exert some control. Thus, the current ripple can be controlled by a proper selection of the inductor.

Let us now analyze the circuit when the switch is in its open position. The inductor current completes its path through the lower side MOSFET and the corresponding differential equation, for $0 \le t \le T_{OFF}$, is

$$L \frac{di_L(t)}{dt} = -V_o \qquad \text{(Eq. 4-8)}$$

From the solution of the above first-order differential equation, we obtain

$$i_L(t) = -\frac{V_o}{L} t + I_{L,\max} \qquad \text{(Eq. 4-9)}$$

Where $I_{L,\max}$ is the maximum value of the current in the inductor at the opening of the switch or the beginning of the off period. As $t \to T_{OFF} = (1-D)T$, the inductor current decreases to its minimum value $I_{L,\min}$ such that

$$I_{L,\min} = -\frac{V_o}{L}(1-D)T + I_{L,\max} \qquad \text{(Eq. 4-10)}$$

The Eq. 4-10 yields another expression for the peak-to-peak current ripple as

$$\Delta I_L = I_{L,\max} - I_{L,\min} = \frac{V_o}{L}(1-D)T \qquad \text{(Eq. 4-11)}$$

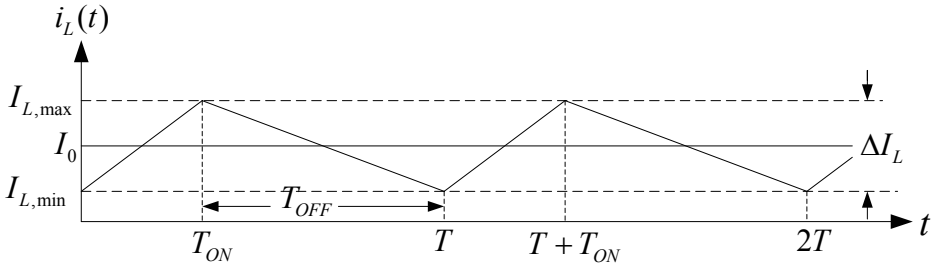

Figure 19: Inductor Current

The current through the inductor as given by Eq. 4-5 during the on time and by Eq. 4-9 during the off time is sketched in the Figure 19. The average current in the inductor must be equal to the dc current through the load. That is,

$$I_{L,avg} = I_o = \frac{V_o}{R} \qquad \text{(Eq. 4-12)}$$

The expressions for the maximum and minimum currents through the inductor may now be written as

$$I_{L,\max} = I_{L,avg} + \frac{\Delta I_L}{2} = \frac{V_o}{R} + \frac{V_o}{2L}(1-D)T \qquad \text{(Eq. 4-13)}$$

$$I_{L,\min} = I_{L,avg} - \frac{\Delta I_L}{2} = \frac{V_o}{R} - \frac{V_o}{2L}(1-D)T \qquad \text{(Eq. 4-14)}$$

The current supplied by the source varies from $I_{L,\min}$ to $I_{L,\max}$ during the time the switch is closed and is zero otherwise as shown in Figure 20.

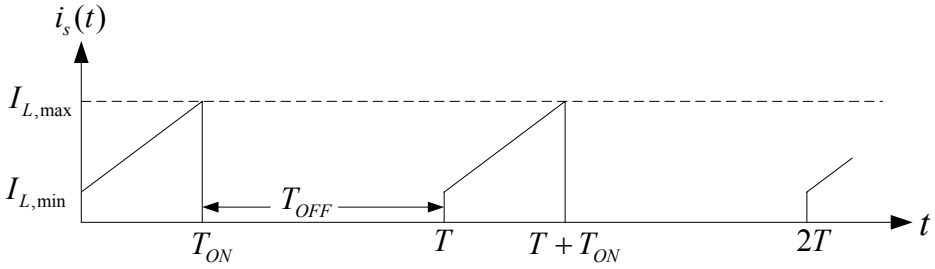

Figure 20: The source current

When the switch, the inductor, and the capacitor are treated as ideal elements, the average power dissipated by them is zero. Consequently, the average power supplied by the source must be equal to the average power delivered to the load. That is,

$$V_d I_d = V_o I_o = D V_S I_o \qquad \text{(Eq. 4-15)}$$

This equation helps us express the average source current in terms of the average load current as

$$I_S = D I_o \qquad \text{(Eq. 4-16)}$$

The current through the lower side MOSFET is shown in Figure 21. Its average value is

$$I_{LS} = (1 - D) I_o \qquad \text{(Eq. 4-17)}$$

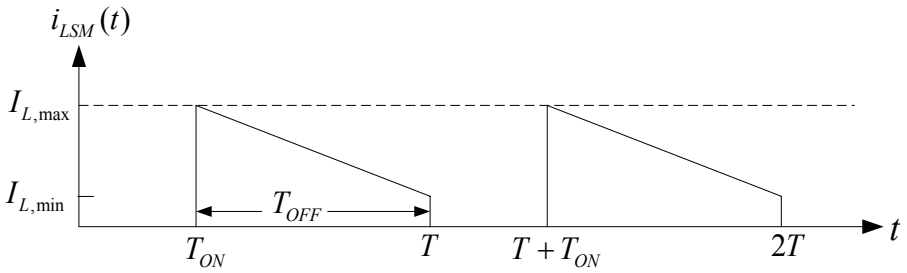

Figure 21: Current through the low side MOSFET

We know the fact that the buck converter can either operate in its continuous conduction mode or discontinuous mode. When it operates in the continuous conduction mode, there is always a current in the inductor. The minimum current in the continuous conduction mode can be zero. Consequently, there is a minimum value of the inductor that ensures its continuous conduction mode. It can be obtained from Eq. 4-14 by setting $I_{L,\min}$ to zero as

$$\frac{V_o}{R} - \frac{V_o}{2L_{\min}}(1 - D)T = 0 \qquad \text{(Eq. 4-18)}$$

Hence,

$$L_{\min} = \frac{1 - D}{2} RT = \frac{1 - D}{2f} R \qquad \text{(Eq. 4-19)}$$

4.3 Calculation for Capacitor

The output capacitor is assumed to be so large as to yield $v_o(t) = V_o$. However, the ripple in the output voltage with a practical value of capacitance can be calculated by considering the waveforms shown in Figure 22 for a continuous-conduction mode of operation. Assuming that all of the ripple component in i_L flows through the capacitor and its average component flows through the load resistor, the shaded area in Figure 22 represents an additional charge ΔQ.

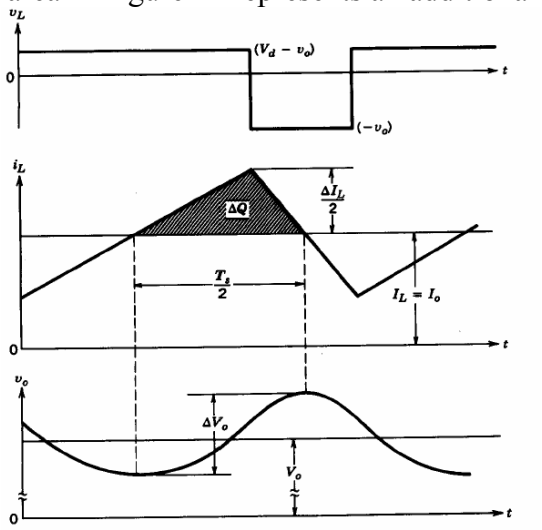

Figure 22: Output voltage ripple in a step-down converter

Therefore, the peak-to-peak voltage ripple ΔV_o can be written as

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{1}{C}\frac{1}{2}\frac{\Delta I_L}{2}\frac{T_s}{2} \qquad \text{(Eq. 4-20)}$$

From Figure 22 during t_{off}

$$\Delta I_L = \frac{V_o}{L}(1-D)T_s \qquad \text{(Eq. 4-23)}$$

Therefore, substituting ΔI_L from Eq. 4-23 into the Eq. 4-20 gives

$$\Delta V_o = \frac{T_s}{8C}\frac{V_o}{L}(1-D)T_s \qquad \text{(Eq. 4-24)}$$

$$\therefore \frac{\Delta V_o}{V_o} = \frac{1}{8}\frac{T_s^2(1-D)}{LC} = \frac{\pi^2}{2}(1-D)\left(\frac{f_c}{f_s}\right)^2 \qquad \text{(Eq. 4-25)}$$

Where switching frequency $f_s = 1/T_s$ and

$$f_c = \frac{1}{2\pi\sqrt{LC}} \qquad \text{(Eq. 4-26)}$$

Equation 4-25 shows that the voltage ripple can be minimized by selecting a corner frequency f_c of the low pass filter at the output such that $f_c << f_s$. Also, the ripple is independent of the output load power, so long as the converter operates in the continuous-conduction mode. We should note that in switch-mode dc power supplies, the percentage ripple in the output voltage is usually specified to be less than, for instance, 1%.

The analysis carried out above assumes ideal components and if we were to make the analysis using all the non-ideal components it would make the derivation a bit more complex with a lot of other parameters included in the final equation. But for the calculation of initial values of the components the above approximations does result in reasonable values. It is also important to realize here that the ESR and ESL are also important and can even dominate. More about how the non-ideality can affect the overall system can be found on [21].

4.4 PWM Controller

The heart of a switching power supply is its switch control circuit (controller). One of the key objectives in designing a controller for the power converter is to obtain tight output voltage regulation under different line and load conditions [7]. Often, the control circuit is a negative-feedback control loop connected to the switch through a comparator and a Pulse Width Modulator (PWM). The switch control signal (PWM), controls the state (on or off) of the switch. This control circuit regulates the output voltage against changes in the load and the input voltage.

4.4.1 PWM

PWM is the method of choice to control modern power electronics circuits. The basic idea is to control the duty cycle of a switch such that a load sees a controllable average voltage. To achieve this, the switching frequency (repetition frequency for the PWM signal) is chosen high enough that the load

cannot follow the individual switching events and they appear just a "blur" to the load, which reacts only to the average state of the switch (later on in this chapter the State Space Averaging Method will be introduced).

With pulse-width modulation control, the regulation of output voltage is achieved by varying the duty cycle of the switch, keeping the frequency of operation constant. Duty cycle refers to the ratio of the period for which the power semiconductor is kept ON to the cycle period. A clearer understanding can be acquired by the Figure 23.

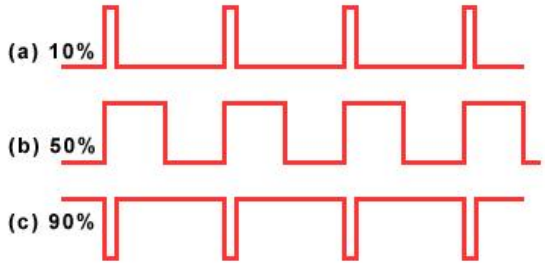

Figure 23: PWM Signal

The Figure 23 shows PWM signals for 10% (a), 50% (b), and 90% (c) duty cycles. Usually control by PWM is the preferred method since constant frequency operation leads to optimization of LC filter and the ripple content in output voltage can be controlled within the set limits.

4.4.2 Comparator and Voltage to PWM Converter

Switching power supplies rely on negative feedback to maintain the output voltages at their specified value. To accomplish this, a differential amplifier is used to sense the difference between an ideal voltage (the reference voltage) and the actual output voltage to establish a small error signal ($v_{control}$).

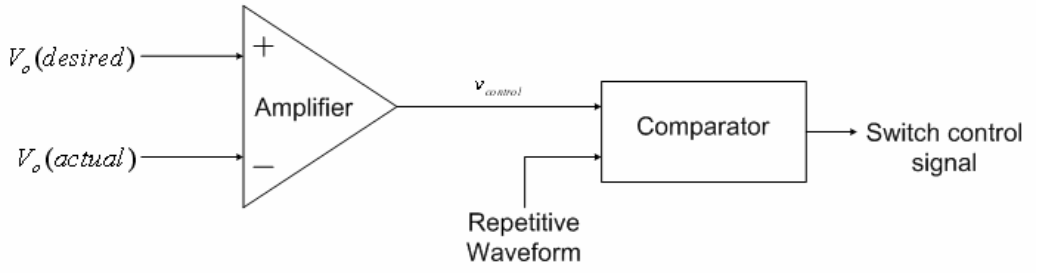

Figure 24: Voltage Reference Comparator [1]

The PWM switching at a constant switching frequency is generated by comparing a signal-level control voltage $v_{control}$ with a repetitive waveform as shown in Figure 24.

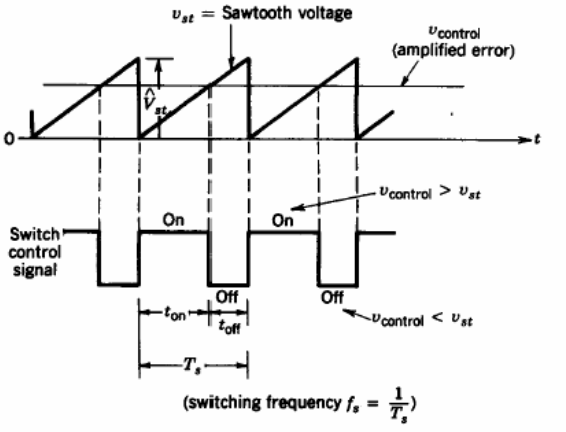

Figure 25: PWM Comparator Signals [1]

The frequency of the repetitive waveform with a constant peak, which is shown to be a sawtooth, establishes the switching frequency. This frequency is kept constant in a PWM control and is chosen to be in a few hundred kilohertz range. When the amplified error signal, which varies very slowly with time relative to the switching frequency, is greater than the sawtooth waveform, the switch control signal becomes HIGH, causing the switch to turn on. Otherwise, the switch is off. So when the circuit output voltage changes, $v_{control}$ also changes causing the comparator threshold to change. Consequently, the output pulse width also changes. This duty cycle change then moves the output voltage to reduce to error signal to zero, thus completing the control loop. In terms of $v_{control}$ and the peak of the sawtooth waveform V_{st} in Figure 25, the switch duty ratio can be expressed as

$$D = \frac{t_{on}}{T_s} = \frac{v_{control}}{\hat{V}_{st}} \qquad \text{(Eq. 4-27)}$$

4.5 Feedback Control System

As has been mentioned earlier as well that the output voltages of dc power supplies are regulated to be within a specified tolerance band (e.g., ±1% around its nominal value) in response to changes in the output load and the input

voltage lines. This process is accomplished by employing a negative feedback system which can be seen in Figure 26.

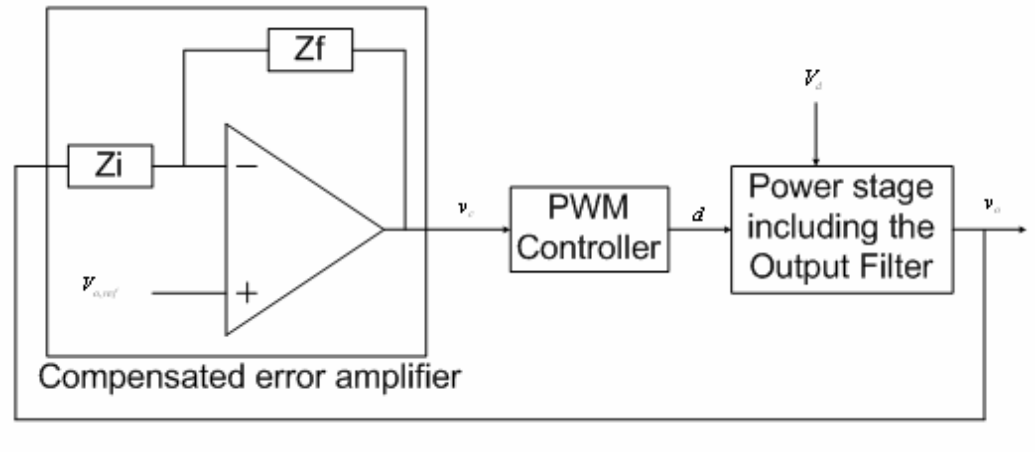

Figure 26: Feedback Control System [1]

The Power stage of the switch converter is not linearized. Since nonlinear systems are not equal to the sum of their parts, they are often difficult (or impossible) to model, and their behaviour with respect to a given variable (for example, time) is extremely difficult to predict. When modelling non-linear systems, therefore, it is common to approximate them as linear, where possible.

With the Linear model, it will make possible certain mathematical assumptions and approximations, allowing for simple computation of results. In nonlinear systems these assumptions cannot be made.

If the power stage of the switch-mode converter in Figure 26 can be linearized, then the Nyquist stability criterion and the Bode plots can be used to determine the appropriate compensation in the feedback loop for the desired steady-state and transient response. Each block in Figure 26 can be linearized around a steady-state operating point as using the state-space averaging technique [5] which allowed the theoretical prediction of a converters frequency response, and therefore a better understanding of a switched-mode regulator's feedback loop and stability criteria. This technique was developed by R. D. Middlebrook at Power Electronics Group - California Institute of Technology, USA. Therefore, each block in Figure 26 can be represented by a transfer function as shown in Figure 27, where the small ac signals are represented by "~."

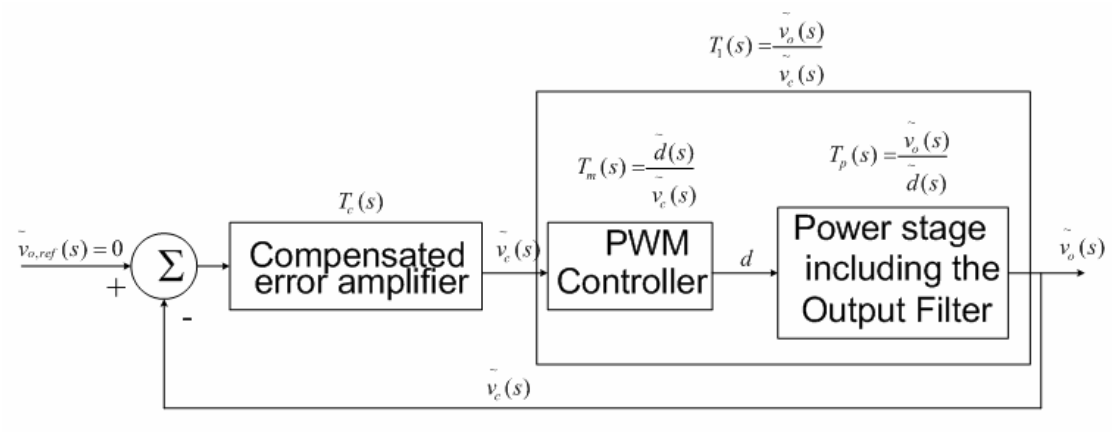

Figure 27: Linearized Feedback Control System [1]

4.6 Linearization using State-Space Averaging

The goal of the following analysis is to obtain a small signal transfer function $\tilde{v}_o(s)/\tilde{d}(s)$, where $\tilde{v}_o$ and $\tilde{d}$ are small perturbations in the output voltage v_o and the switch duty ratio *d*, respectively, around their steady-state dc operating values V_o and D [1].

4.6.1 Power Stage & Output Filter

Step 1 State-Variable Description for Each Circuit State. In a converter operating in a continuous-conduction mode, there are two circuit states: one state corresponds to when the switch is on and the other to when the switch is off. A third circuit state exists during the discontinuous interval, which is not considered in the following analysis because of the assumption of a continuous-conduction mode of operation.

During each circuit state, the linear circuit is described by means of the state-variable vector **x** consisting of the inductor current and the capacitor voltage. In the circuit description, the parasitic elements such as the resistance of the filter inductor and the equivalent series resistance (ESR) of the filter capacitor should also be included. Here V_d is the input voltage. A lowercase letter is used to represent a variable, which includes its steady-state dc value plus a small ac perturbation, for example, $v_o = V_o + \tilde{v}_o$. Therefore, during each circuit state, we can write the following state equations:

$$\dot{\mathbf{x}} = \mathbf{A}_1\mathbf{x} + \mathbf{B}_1 v_d \qquad \text{during } d \cdot T_s \qquad \text{(Eq. 4-28)}$$

and

$$\dot{\mathbf{x}} = \mathbf{A}_2\mathbf{x} + \mathbf{B}_2 v_d \qquad \text{during } (1-d)\cdot T_s \qquad \text{(Eq. 4-29)}$$

where $\mathbf{A}_1$ and $\mathbf{A}_2$ are state matrices and $\mathbf{B}_1$ and $\mathbf{B}_2$ are vectors.

The output v_o in all converters can be described in terms of their state variables alone as

$$v_o = \mathbf{C}_1\mathbf{x} \qquad \text{during } d\cdot T_s \qquad \text{(Eq. 4-30)}$$

and

$$v_o = \mathbf{C}_2\mathbf{x} \qquad \text{during } (1-d)\cdot T_s \qquad \text{(Eq. 4-31)}$$

where $\mathbf{C}_1$ and $\mathbf{C}_2$ are transposed vectors.

Step 2 Averaging the State-Variable Description Using the Duty Ratio *d*. To produce an average description of the circuit over a switching period, the equations corresponding to the two foregoing states are time weighted and averaged, resulting in the following equations:

$$\dot{\mathbf{x}} = [\mathbf{A}_1 d + \mathbf{A}_2(1-d)]\mathbf{x} + [\mathbf{B}_1 d + \mathbf{B}_2(1-d)]v_d \qquad \text{(Eq. 4-32)}$$

and

$$v_o = [\mathbf{C}_1 d + \mathbf{C}_2(1-d)]\mathbf{x} \qquad \text{(Eq. 4-33)}$$

Step 3: Introducing Small ac Perturbations and Separation into ac and dc Components. Small ac perturbations, represented by "~", are introduced in the dc steady-state quantities (which are represented by the upper case letters). Therefore,

$$\mathbf{x} = \mathbf{X} + \tilde{\mathbf{x}} \qquad \text{(Eq. 4-34)}$$

$$v_o = V_0 + \tilde{v}_o \qquad \text{(Eq. 4-35)}$$

and

$$d = D + \tilde{d} \qquad \text{(Eq. 4-36)}$$

In general, $v_d = V_d + \tilde{v}_d$. However, in view of our goal to obtain the transfer function between voltage $\tilde{v}_o$ and the duty ratio $\tilde{d}$, the perturbation $\tilde{v}_d$ is assumed to be zero in the input voltage to simplify our analysis. Therefore

$$v_d = V_d \qquad \text{(Eq. 4-37)}$$

Using Eq. 4-34 through 4-37 in Eq 4-32 and recognizing that in steady state, $\dot{\mathbf{X}} = 0$,

$$\dot{\tilde{\mathbf{x}}} = \mathbf{AX} + \mathbf{B}V_d + \mathbf{A}\tilde{\mathbf{x}} + \left[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)V_d\right]\tilde{d} + \text{terms containing products}$$

of $\tilde{\mathbf{x}}$ and $\tilde{d}$ (to be neglected) (Eq. 4-38)

where

$$\mathbf{A} = \mathbf{A}_1 D + \mathbf{A}_2(1 - D) \quad \text{(Eq. 4-39)}$$

and

$$\mathbf{B} = \mathbf{B}_1 D + \mathbf{B}_2(1 - D) \quad \text{(Eq. 4-40)}$$

The steady-state equation can be obtained from Eq. 4-38 by setting all the perturbation terms and their derivatives to zero. Therefore, the steady-state equation is

$$\mathbf{AX} + \mathbf{B}V_d = 0 \quad \text{(Eq. 4-41)}$$

and therefore in Eq. 4-38

$$\dot{\tilde{\mathbf{x}}} = \mathbf{A}\tilde{\mathbf{x}} + \left[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)V_d\right]\tilde{d} \quad \text{(Eq. 4-42)}$$

Similarly, usings Eqs. 4-34 to 4-36 in Eq. 4-33 results in

$$V_o + \tilde{v}_o = \mathbf{CX} + \mathbf{C}\tilde{\mathbf{x}} + \left[(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X}\right]\tilde{d} \quad \text{(Eq. 4-43)}$$

where

$$\mathbf{C} = \mathbf{C}_1 D + \mathbf{C}_2(1 - D) \quad \text{(Eq. 4-44)}$$

In Eq. 4-43, the steady-state output voltage is given as

$$V_o = \mathbf{CX} \quad \text{(Eq. 4-45)}$$

and therefore,

$$\tilde{v}_o = \mathbf{C}\tilde{\mathbf{x}} + \left[(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X}\right]\tilde{d} \quad \text{(Eq. 4-46)}$$

Using Eqs. 4-41 and 4-45, the steady-state dc voltage transfer function is

$$\frac{V_o}{V_d} = -\mathbf{CA}^{-1}\mathbf{B} \quad \text{(Eq.4-47)}$$

Step 4: Transformation of the ac Equations in to *s*-Domain to Solve for the Transfer Function. Equations 4-42 and 4-46 consist of the ac perturbations. Using Laplace transformation in Eq 4-42,

$$s\tilde{\mathbf{x}}(s) = \mathbf{A}\tilde{\mathbf{x}}(s) + \left[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)V_d\right]\tilde{d}(s) \qquad \text{(Eq. 4-48)}$$

or

$$\tilde{\mathbf{x}}(s) = \left[s\mathbf{I} - \mathbf{A}\right]^{-1}\left[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)V_d\right]\tilde{d}(s) \qquad \text{(Eq. 4-49)}$$

Where **I** is a unity matrix. Using a Laplace transformation in Eq. 4-46 and expressing in terms $\tilde{\mathbf{x}}(s)$ in terms of $\tilde{d}(s)$ from Eq. 4-49 results in the desired transfer function $T_p(s)$ of the power stages:

$$T_p(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \mathbf{C}\left[s\mathbf{I} - \mathbf{A}\right]^{-1}\left[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)V_d\right] + (\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} \quad \text{(Eq. 4-50)}$$

Buck Converter

Now we will linearize the power stage and the output filter of the Buck Converter given in Figure 28. The two switches are represented by diodes.

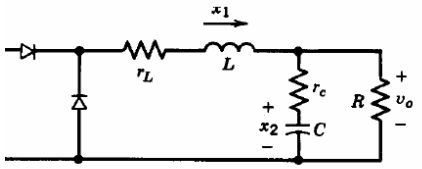

Figure 28: Buck Converter Circuit [1]

r_L is inductor resistance, r_c is the equivalent series resistance of the capacitor, and R is the load resistance.

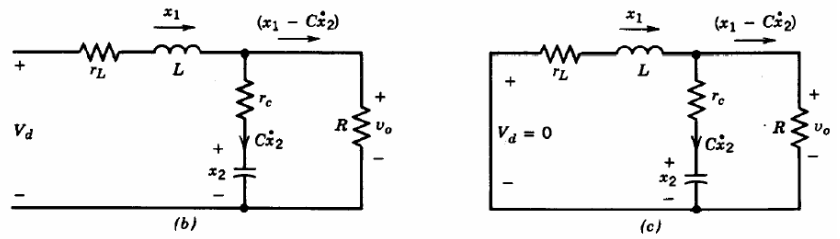

Figure 29: Buck Converter (a) switch on; (b) switch off [1]

From Figure 29 the following equations can be derived (See Appendix F for Linear Differential Equations).

$$-V_d + L\dot{x}_1 + r_L x_1 + R(x_1 - C\dot{x}_2) = 0 \qquad \text{(Eq. 4-51)}$$

and

$$-x_2 - Cr_c\dot{x}_2 + R(x_1 - C\dot{x}_2) = 0 \qquad \text{(Eq. 4-52)}$$

In matrix form, these two equations can be written as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -\dfrac{Rr_c + Rr_L + r_c r_L}{L(R+r_c)} & -\dfrac{R}{L(R+r_c)} \\ \dfrac{R}{C(R+r_c)} & -\dfrac{1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} V_d \qquad \text{(Eq. 4-53)}$$

Comparing the equations with Eq. 4-28 yields

$$\mathbf{A}_1 = \begin{bmatrix} -\dfrac{Rr_c + Rr_L + r_c r_L}{L(R+r_c)} & -\dfrac{R}{L(R+r_c)} \\ \dfrac{R}{C(R+r_c)} & -\dfrac{1}{C(R+r_c)} \end{bmatrix} \qquad \text{(Eq. 4-54)}$$

and

$$\mathbf{B}_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} \qquad \text{(Eq. 4-55)}$$

The state equation for the circuit of Fig 4-12c with the switch off can be written by observation, noting that the circuit of Fig. 4-12c is exactly the same as the circuit of Fig 4-12b with V_d set to zero.

$$\mathbf{A}_2 = \mathbf{A}_1 \qquad \text{(Eq. 4-56)}$$

$$\mathbf{B}_2 = 0 \qquad \text{(Eq. 4-57)}$$

The output voltage in both the circuit states is given as

$$\begin{aligned} v_o &= R(x_1 - C\dot{x}_2) \qquad \text{(Eq. 4-58)} \\ &= \frac{Rr_c}{R+r_c}x_1 + \frac{R}{R+r_c}x_2 \end{aligned}$$

Using $\dot{x}_2$ from Eq. 4-52

$$= \begin{bmatrix} \frac{Rr_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

Therefore, in Eq. 4-30 and 4-31

$$\mathbf{C}_1 = \mathbf{C}_2 = \begin{bmatrix} \frac{Rr_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \quad \text{(Eq. 4-59)}$$

$$\mathbf{A} = \mathbf{A}_1 \text{ (from Eq. 4-39 and Eq. 4-56)} \quad \text{(Eq. 4-60)}$$

$$\mathbf{B} = \mathbf{B}_1 D \text{ (from Eq. 4-40 and Eq. 4-57)} \quad \text{(Eq. 4-61)}$$

$$\mathbf{C} = \mathbf{C}_1 \text{ (from Eq. 4-44 and Eq. 4-59)} \quad \text{(Eq. 4-62)}$$

Model Simplification

In all practical circuits,

$$R >> (r_c + r_L) \quad \text{(Eq. 4-63)}$$

Therefore, **A** and **C** are simplified as

$$\mathbf{A} = \mathbf{A}_1 = \mathbf{A}_2 = \begin{bmatrix} -\frac{r_c + r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \quad \text{(Eq. 4-64)}$$

$$\mathbf{C} = \mathbf{C}_1 = \mathbf{C}_2 \cong \begin{bmatrix} r_c & 1 \end{bmatrix} \quad \text{(Eq. 4-65)}$$

and **B** remains unaffected as

$$\mathbf{B} = \mathbf{B}_1 D = \begin{bmatrix} 1/L \\ 0 \end{bmatrix} D \quad \text{(Eq. 4-66)}$$

Where $\mathbf{B}_2$=0. From Eq. ,

$$\mathbf{A}^{-1} = \frac{LC}{1 + (r_c + r_L)/R} \begin{bmatrix} -\frac{1}{CR} & \frac{1}{L} \\ -\frac{1}{C} & -\frac{r_c + r_L}{L} \end{bmatrix} \quad \text{(Eq. 4-67)}$$

$$\frac{V_o}{V_d} = D\frac{R + r_c}{R + (r_c + r_L)} \cong D \qquad \text{(Eq. 4-68)}$$

$$T_p(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} \cong V_d \frac{1 + sr_cC}{LC\left\{s^2 + s\left[1/CR + (r_c + r_L)/L\right] + 1/LC\right\}} \qquad \text{(Eq. 4-69)}$$

Eq. 4-69 is the Open Loop Transfer Function of the circuit represented in Figure 29. The term in the curly brackets in the denominator of Eq. 4-69 are of the form $s^2 + 2\xi\omega_o s + \omega_0^2$, where

$$\omega_o = \frac{1}{\sqrt{LC}} \qquad \text{(Eq. 4-69)}$$

$$\xi = \frac{1/CR + (r_c + r_L)/L}{2\omega_o} \qquad \text{(Eq. 4-70)}$$

where $\omega_0 = F_{LC}$

Therefore, from Eq. 4-69 the transfer function

$$T_p(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = V_d \frac{\omega_o^2}{\omega_z} \frac{s + \omega_z}{s^2 + 2\xi\omega_o s + \omega_o^2} \qquad \text{(Eq. 4-71)}$$

where a zero is introduced due to the equivalent series resistance of the output capacitor at the frequency

$$\omega_z = F_{ESR} = \frac{1}{r_cC} \qquad \text{(Eq. 4-72)}$$

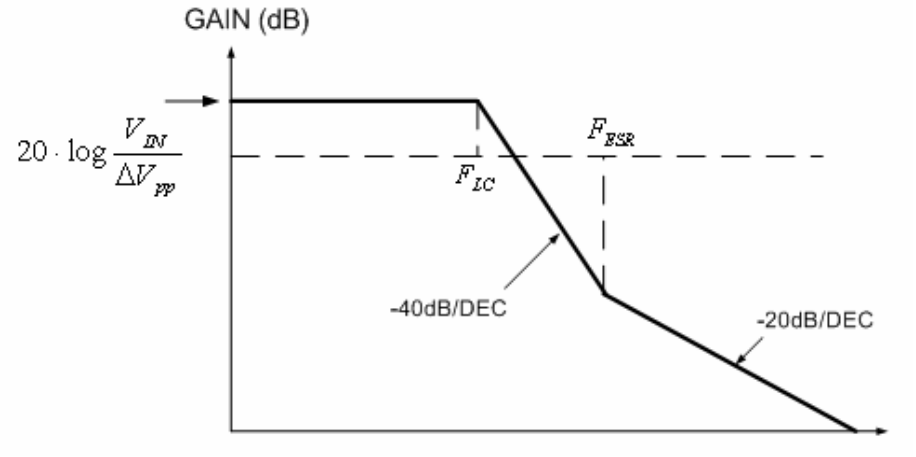

Figure 30: Open Loop System Gain [12]

Figure 30 shows the Bode plot for the transfer function in Eq. 4-71 using the numerical values given in the Fig. It shows the transfer function has a fixed gain and a minimal phase shift at low frequencies. Beyond the resonant frequency $\omega_o = \sqrt{1/LC}$ of the LC output filter, the gain begins to fall with a slope of -40dB/decade and the phase tends toward -180°. At frequencies beyond ω_z, the gain falls with a slope of -20 dB/decade and the phase tends toward -90°. The gain plots shifts vertically with V_d but the phase plot is not affected.

4.6.2 Pulse Width Modulator

In the direct duty ratio pulse-width modulator, the control voltage $v_c(t)$, which is the output of the error amplifier, is compared with a repetitive waveform $v_r(t)$, which establishes the switching frequency f_s, as shown in the Figure 31. The control voltage $v_c(t)$ consists of a dc component and a small ac perturbation component

$$v_c(t) = V_c + \tilde{v}_c(t) \qquad \text{(Eq. 4-73)}$$

Where $v_c(t)$ is in a range between zero and $\hat{V}_r$, as shown in Figure . Here $\tilde{v}_c(t)$ is a sinusoidal ac perturbation in the control voltage at a frequency ω, where ω is much smaller than the switching frequency $\omega_s (= 2\pi f_s)$.

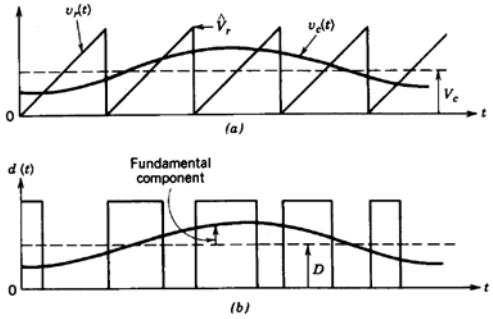

Figure 31: Pulse-width modulator [1]

The ac perturbation in the control voltage can be expressed as

$$\tilde{v}_c(t) = a\sin(\omega t - \phi) \qquad \text{(Eq. 4-74)}$$

by means of an amplitude *a* and an arbitrary phase angle φ.

In Figure 31, the instantaneous switch duty ratio *d(t)* is as follows:

$$d(t) = \begin{cases} 1.0 \\ 0 \end{cases} \qquad \text{(Eq.4-75/7}$$

The sinusoidal PWM can be expressed in terms of the Fourier series as

$$d(t) = \frac{V_c}{\hat{V}_r} + \frac{a}{\hat{V}_r}\sin(\omega t - \phi) + other\ high\ \ frequency\ \ components \qquad \text{(Eq. 4-78)}$$

The higher frequency components in the output voltage v_o due to the high-frequency components in *d(t)* are eliminated because of the low-pass filter at the output of the converter. Therefore, the high-frequency components in Eq. 4-78 can be ignored. In terms of its dc value and its ac perturbation

$$d(t) = D + \tilde{d}(t) \qquad \text{(Eq. 4-79)}$$

Comparing Eq. 4-78 and 4-79 yields

$$D = \frac{V_c}{\hat{V}_r} \qquad \text{(Eq. 4-80)}$$

and

$$\tilde{d}(t) = \frac{a}{\hat{V}_r}\sin(\omega t - \phi) \qquad \text{(Eq. 4-81)}$$

From Eqs. 4-74 and 4-81, the transfer function $T_m(s)$ of the modulator is given by

$$T_m(s) = \frac{\tilde{d}(s)}{\tilde{v}_c(s)} = \frac{1}{\hat{V}_r} \qquad \text{(Eq. 4-82)}$$

4.7 Stability Criteria

It is the desire of all designers of power supplies, whether they are switching or not, for accurate and tight regulation of the output voltage(s). To accomplish regulation we need to add a feedback loop. The feedback loop can cause an otherwise stable system to become unstable. Even though the transfer function of the original converter might not contain any right hand poles but after feedback it is possible that right hand poles may be introduced. Also we need to introduce a high DC gain. But with high gain again comes the possibility of instability.

These two issues determine the need to have stability criteria for a power supply. Hence, feedback compensation design involves selection of a suitable compensation circuit configuration and positioning of its poles and zeros to yield an open loop transfer function. Certain very important parameters need to be taken in to account when calculating the stability of the power supply.

- Variations in input voltage do not cause instability.
- Allow for variations in the peak-to-peak oscillator voltage.
- Error amplifier (which we will discuss in the next section) has sufficient attenuation at the switching frequency so that it does not amplify the output voltage ripple and cause sub-harmonic oscillations.
- Mid-frequency gain is greater than zero to prevent a large overshoot at turn-on and during transient conditions.
- Error amplifier has the drive capability to drive the feedback network properly.
- High gain at low frequency region to provide tight output voltage regulation and minimize the steady-state error in the power supply output.
- The phase margin determines the transient response of the output voltage in response to sudden changes in the load and the input voltage. The difference between 180° and the actual phase when the gain reaches unity gain. (In this case it is approaching zero.) Phase margins of 45º to 60º (360º degree minus the total closed-loop phase lag) are considered safe values that yield well-damped transient load responses. The recommended value is 45° to 60° [1].
- Gain Margin is the difference between unity gain (zero dB) and the actual gain when the phase reaches 180°. (In this case it is a positive number.) The recommended value is -6dB to -12 dB.
- A crossover frequency (or bandwidth), f_c, of between one tenth and one fourth of a switching frequency for a system to respond sufficiently fast to transients, such as a sudden change of load.

A commonly used derivative from the above definitions is that if the slope of the gain response as it crosses the unity-gain axis is not more than -20 dB / decade, the phase margin will be greater than 45° and the system will be stable.

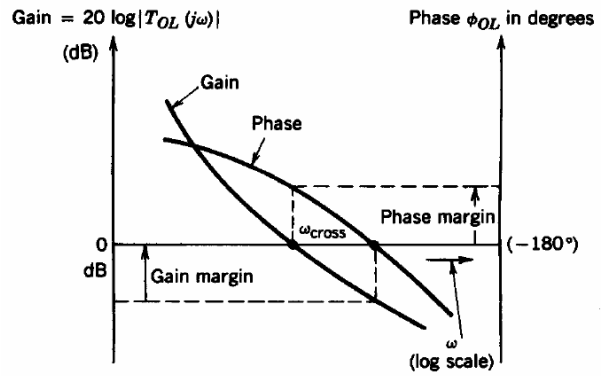

Figure 32: Definitions of the crossover frequency, phase and gain margins [1]

4.8 Compensator

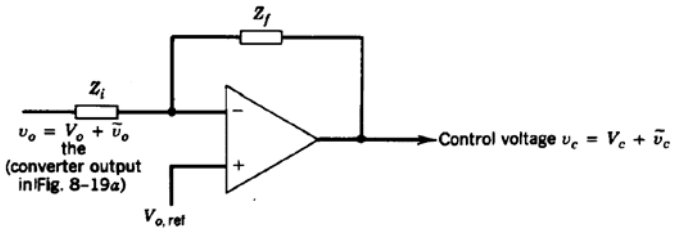

Figure 33: A general compensated error amplifier [1]

After the values for external filter components are chosen (according to our requirements) than only the power stage is complete. The original filter of the buck converter by itself has a very low phase margin which needs to be increased. A better phase margin can be included by adding a suitable controller in a closed loop configuration [28]. Proper compensation of the system will allow for a predictable bandwidth with unconditional stability. In most cases, a Type II or Type III compensated network will properly compensate the system. The ideal Bode plot for the compensated system would be a gain that rolls off at a slope of -20dB/decade, crossing 0db at the desired bandwidth and a phase margin greater than 45° for all frequencies below the 0dB crossing [12].

According to [13] the designer must compensate the power supply to ensure that the overall loop response is stable. The purpose of adding compensation to the error amplifier is to counter act some of the gains and phases contained in the control-to-output transfer function that could jeopardize the stability of the power supply. Obviously, the ultimate goal is to make the overall closed loop transfer function (control-to-output cascaded with the error amplifier) satisfy the stability criteria. This is to avoid having the closed-loop phase any closer to 360º

than the desired phase margin anywhere where the gain is greater than 1 (0 dB). It is also desirable to have the slope of the gain curve at the crossover point with a value of -20 dB/decade. The overall frequency-response loop has two parts. The first includes a power-stage with driver and PWM comparator and the second is the compensation. The compensation circuit based on an error-amplifier with the R and C external components shapes the required feedback-loop frequency response.

4.8.1 Type I Compensation

Dominant pole compensations, or single pole compensation, are referred to as a Type I Compensation [25]. This type of compensation is used for converter topologies that exhibit a minimal phase shift prior to the anticipated gain crossover point. These include forward-mode regulators such as the buck, push-pull, and half- and full-bridge using either voltage or current mode control techniques. These converters exhibit a relatively low phase shift below the pole contributed by the output filter. This compensation yields, though, a relatively poor transient response time because the gain crossover frequency occurs at a low frequency. Its load regulation is very good, though, since its DC gain is very high.

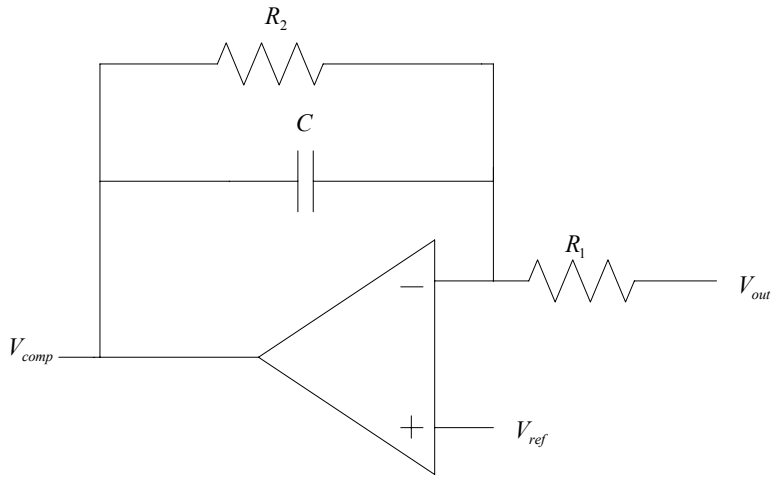

Figure 34: Type I Compensation [13]

$$K(s) = \frac{-V_{out}(s)}{V_{in}(s)} = \frac{R_2}{R_1(1 + R_2 C_2 s)} \qquad \text{(Eq. 4-83)}$$

This method of error amplifier compensation is generally not used if a rapid transient load response time is desired. The methods for calculating the values of

R_1 and R_2 on the basis of which the function can be designed are mentioned in [12].

4.8.2 Type II Compensation

The Type II network helps to shape the profile of the gain with respect to frequency and also gives a 90° boost to the phase. This boost is necessary to counteract the effects of the resonant output filter at the double pole [12].

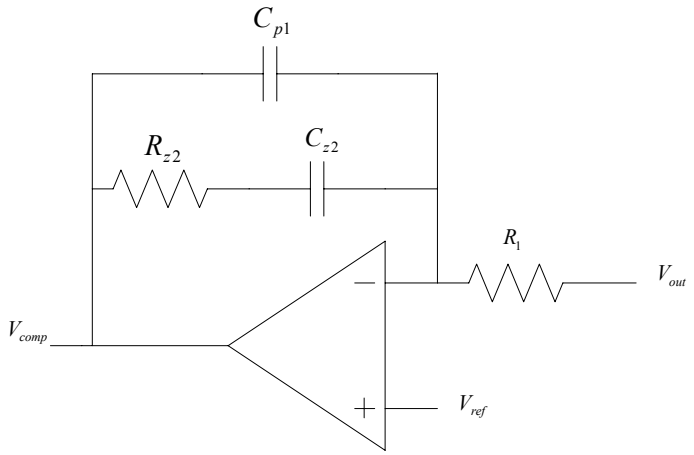

Figure 35: Type II Compensation

$$GAIN_{TYPEII} = \frac{1}{R_1 C_{p1}} \cdot \frac{\left(s + \frac{1}{R_{z2} \cdot C_{z2}}\right)}{s \cdot \left(s + \frac{C_{p1} + C_{z2}}{R_2 \cdot C_1 \cdot C_2}\right)} \qquad \text{(Eq. 4-84)}$$

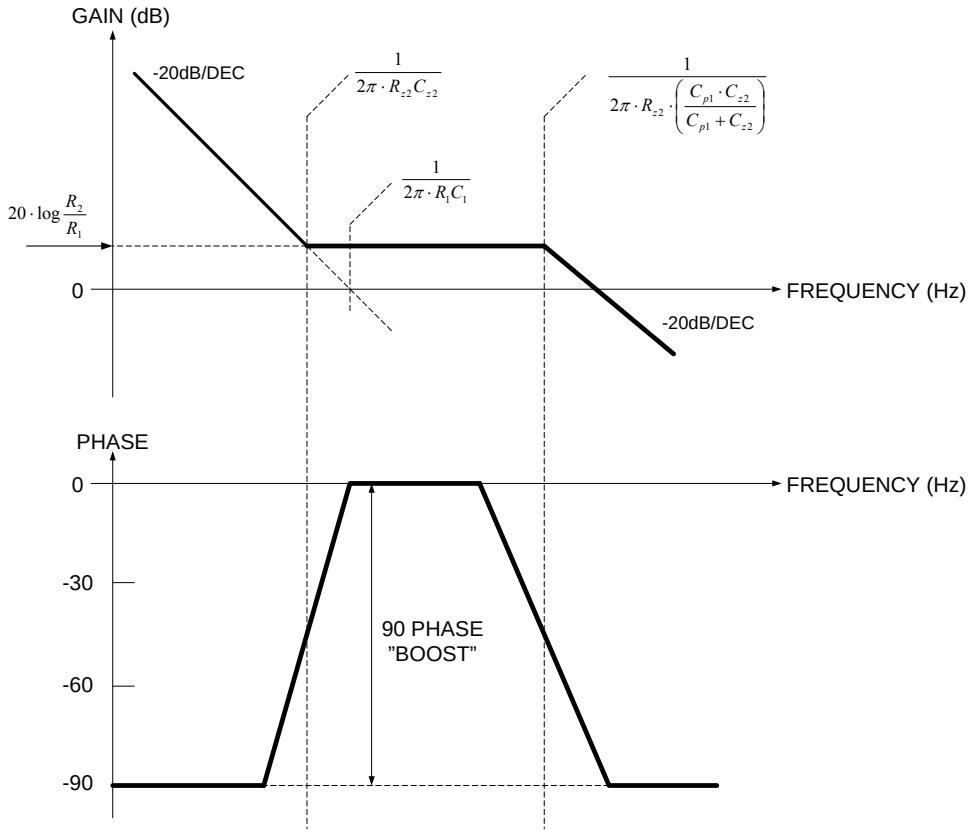

Figure 36: Generic Type II Network

To calculate the values of poles and zeroes, and from those the component values, for a Type II network we will use the guidelines provided by [12].

1. Choose a value for R_1 (a higher value R_1 will result in a lower value of C & vice versa)
2. Select a gain (R_2 / R_1) that will shift the Open Loop Gain up to give the desired bandwidth (DBW). This will allow the 0dB crossover to occur in the frequency range where the Type II network has a flat gain. The following equation will calculate an R_2, that will accomplish this given the system parameters and a chosen R_1.

$$R_2 = \left(\frac{F_{ESR}}{F_{LC}} \right)^2 \cdot \frac{DBW}{F_{ESR}} \cdot \frac{\Delta V_{OSC}}{V_{IN}} \cdot R_1 \qquad \text{(Eq. 4-85)}$$

From Eq. 4-69, we can calculate the value of F_{LC}:

$$F_{LC} = \frac{1}{2\pi\sqrt{LC}} \quad \text{(Eq. 4-86)}$$

From Eq. 4-72, we can calculate the value of F_{ESR}:

$$F_{ESR} = \frac{1}{2\pi r_C C} \quad \text{(Eq. 4-87)}$$

$$DBW = 0.3 \times f_{sw} \quad \text{(Eq. 4-88)}$$

3. Calculate C_2 by placing the zero a decade below the output filter double pole frequency:

$$C_2 = \frac{10}{2\pi \cdot R_2 \cdot F_{LC}} \quad \text{(Eq. 4-89)}$$

4. Calculate C_1 by placing the second pole at half the switching frequency:

$$C_1 = \frac{C_2}{(\pi \cdot R_2 \cdot C_2 \cdot f_{sw}) - 1} \quad \text{(Eq. 4-90)}$$

This type of compensation can only be used in converters where output filter capacitor has a relatively high ESR. Where output capacitor ESR is low a Type III Compensation is usually necessary [23]. Type II Compensator used to compensate a first-order filter, usually from a current-mode converter [26].

4.8.3 Type III Compensation

Type III network shapes the profile of the gain with respect to frequency in a similar fashion to the Type II network, but utilizes two zeroes to give a phase boost of 180°. This boost is necessary to counteract the effects of an under damped resonance of the output filter at the double pole. The Type III compensation circuit has two poles, with two zeros and a pole at its origin providing an integration function for better DC accuracy. Optimal selection of the compensation circuit depends on the power-stage frequency response.

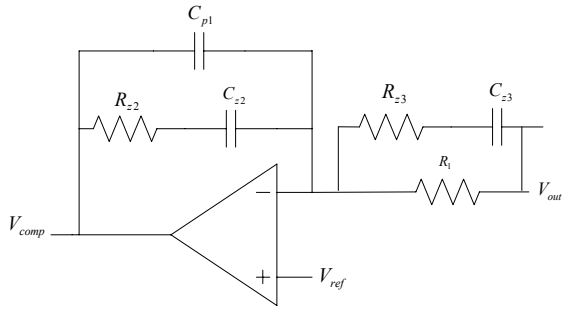

Figure 37: Type III Compensation

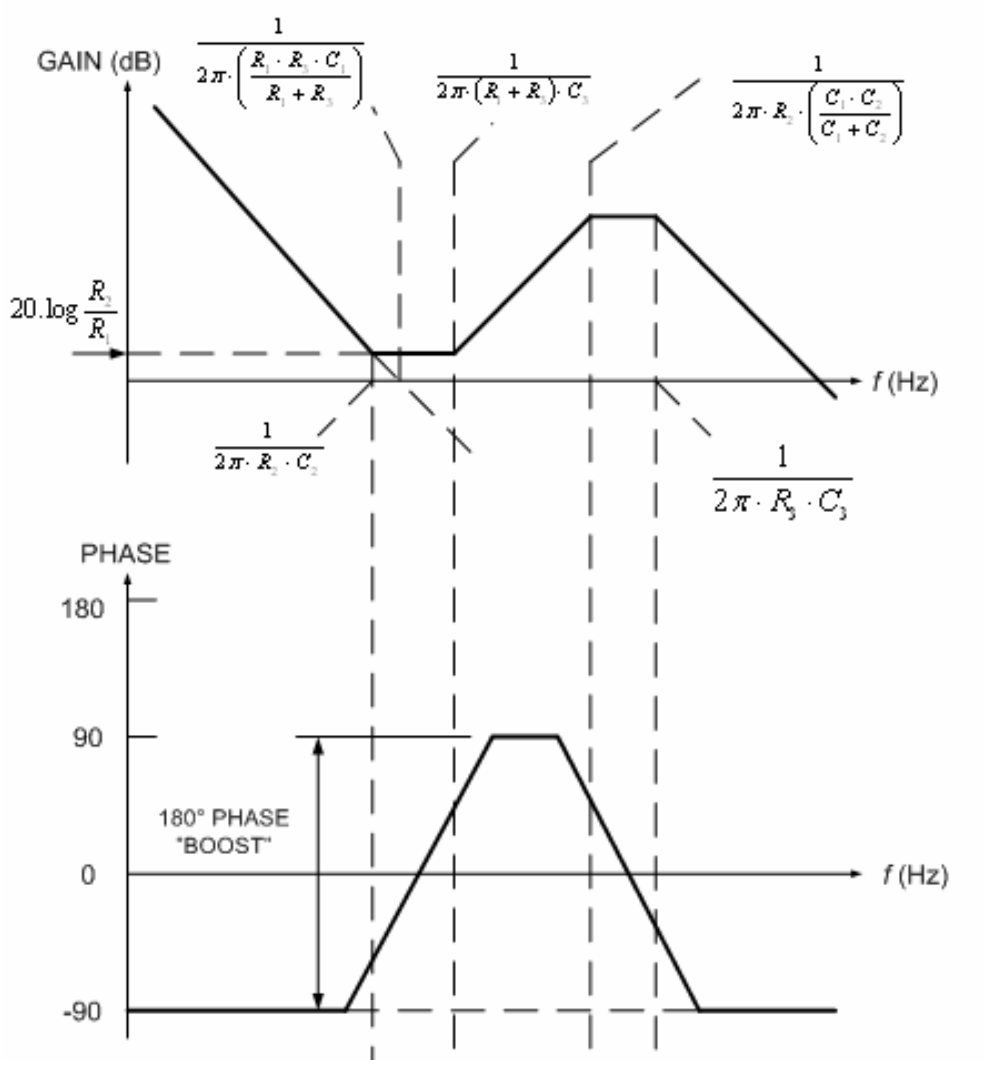

Figure 38: Generic Type III Network

$$GAIN_{TYPEIII} = \frac{R_1 + R_{z3}}{R_1 \cdot R_{z3} \cdot C_{p1}} \cdot \frac{\left(s + \frac{1}{R_{z2} \cdot C_{z2}}\right) \cdot \left(s + \frac{1}{(R_1 + R_{z3}) \cdot C_{z3}}\right)}{s \cdot \left(s + \frac{C_1 + C_{z2}}{R_{z2} \cdot C_{p1} \cdot C_{z2}}\right) \cdot \left(s + \frac{1}{R_{z3} \cdot C_{z3}}\right)} \quad \text{(Eq. 4-91)}$$

There are certain guidelines from [12] that can be used for positioning the poles and zeros and for calculating the component values.

1. Choose a value of R_1
2. Select a gain (R_2 / R_1) that will shift the Open Loop Gain up to give the desired bandwidth. This will allow the 0dB crossover to occur in the frequency range where the Type III network has its second flat gain. The following equation will calculate an R_2, that will accomplish this given the system parameters and a chosen R_1.

$$R_2 = \frac{DBW}{F_{LC}} \cdot \frac{\Delta V_{OSC}}{V_{IN}} \cdot R_1 \quad \text{(Eq. 4-92)}$$

3. Calculate C_2 by placing the zero at 50% of the output filter double pole frequency:

$$C_2 = \frac{1}{\pi \cdot R_2 \cdot F_{LC}} \quad \text{(Eq. 4-93)}$$

4. Calculate C_1 by placing the first pole at the ESR zero frequency:

$$C_1 = \frac{C_2}{\left(2 \cdot \pi \cdot R_2 \cdot C_2 \cdot F_{ESR}\right) - 1} \quad \text{(Eq. 4-94)}$$

5. Set the second pole at half the switching frequency and also set the second zero at the output filter double pole. This combination will yield the following component calculations:

$$R_3 = \frac{R_1}{\left(\frac{f_{sw}}{2 \cdot F_{LC}}\right) - 1} \quad \text{(Eq. 4-95)}$$

$$C_3 = \frac{1}{\pi \cdot R_3 \cdot f_{sw}} \quad \text{(Eq. 4-96)}$$

A traditional type III compensator is sufficient to stabilize the synchronous buck converter for all three modes subsequently being voltage mode control, current mode control & mixed mode control [10]. In the analog design process, Type III compensator is used to compensate a second-order LC filter, usually from a voltage-mode converter [26]. By using Type 3 compensation around the VMC error amplifier when the overall loop performance matches that of a CMC system, albeit at the expense of requiring a higher-bandwidth amplifier [15].

4.9 Feed Forward

One of the basic types of control, the feedback, we have just discussed. Now we shall discuss the feed forward. Feedforward control helps to reduce the influence of input source and switch imperfections on the output voltage. Tied together with a feedback control (controlling unknown disturbances and not having to know exactly how a system will respond to disturbances), feed forward control (responding to disturbances before they can affect the system) can be used to improve a regulator's response to dynamic input variations.

Typically, however, we also want to reduce the error quickly, but inherent with feedback control is the tradeoffs between system response and system stability. The more responsive the feedback network is, the greater becomes the risk of instability.

4.10 Voltage Mode Control / Current Mode Control

The conventional voltage mode control has some disadvantages, such as input voltage dependent loop gain, and slow response to input voltage variations etc. Voltage mode control with input voltage FF (feed forward) can effectively fix all of these weaknesses. Voltage FF is realized by making the slope of the ramp waveform proportional to the input voltage [11]. For a detailed comparison of why VMC is preferred or to compare the advantage [24] can be referred to in detail.

4.10.1 Voltage Mode Control

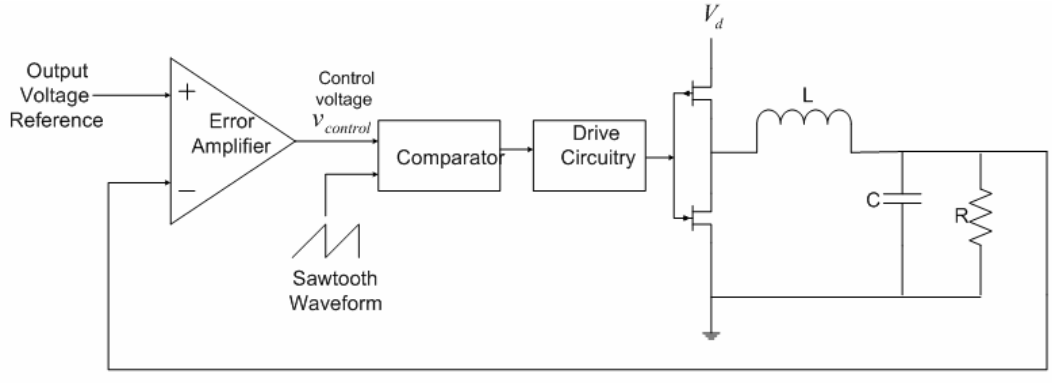

Figure 39: PWM Duty Ratio Control [1]

This is a classical control & simple method in which there is only one feedback from the output voltage. PWM voltage mode controllers have disadvantages. Since the input voltage is a significant parameter in the loop gain, any changes in the input voltage will alter the gain and will change the dynamics of the system. The central issue is that a voltage mode controller alone cannot correct any disturbances or changes until they are detected at the output. In the voltage-based controllers the compensation loop is difficult to implement.

For general purpose single output dc-dc converters, the overall advantage goes with VMC. The feedback network, even with a "Type 3" compensation network around the voltage-error amplifier is relatively simple to compensate. In many ways it is simpler than compensating a current loop, plus a voltage loop, plus adding slop compensation. This, along with the improved noise immunity at light loads, makes VMC attractive from a circuit performance standpoint. [24]

4.10.2 Current Mode Control

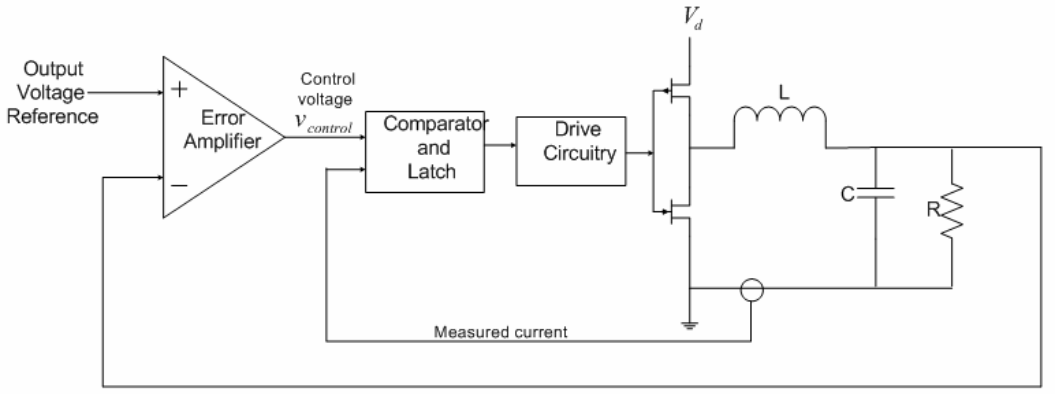

Figure 40: Current Mode Control [1]

In a current-mode control, an additional inner control loop is used as shown in Figure 40, where the control voltage directly controls the output inductor current that feeds the output stage and thus the output voltage. Ideally, the control voltage should act to directly control the *average* value of the inductor for the faster response. The fact that the current feeding the output stage is controlled directly in a current-mode control has a profound effect on the dynamic behaviour of the negative feedback control loop.

Consideration	Voltage Mode	Current Mode
Design	Single loop	Two loops
Transient response	Slower than current mode	Faster than voltage mode
Compensation Techniques	More complex: 3 Poles, 2 Zeros	Less complex: One pole
Current sharing	Requires extra circuitry	Inherent in operation
XFMR flux balancing	Requires extra circuitry	Inherent in operation
Noise immunity	Good	Poor, especially at low loads
Operation at duty cycle >50%	Operates normally	Requires slope compensation beyond 50% duty cycle
Pulse-by-pulse current limiting	Requires current limiting circuitry	Inherent in operation
Loop gain change with VIN	Requires VIN feed-forward circuit	No gain change

Table 2: Voltage Mode vs Current Mode Control [22]

4.11 TradeOffs for Implementation of CMC & VMC

The perceived advantage of CMC is feedback loop response; today's high-frequency VMC controlled converters closely rival their CMC counterparts [24]. Most feedback controllers in buck converters use both the PWM voltage and current mode controllers to produce a better steady-state response and to reduce the voltage overshoots during start-ups.

5. Designing a practical Buck Converter

Factors to consider when deciding on a regulated voltage supply solution include:

- Available source input voltage
- Desired supply output voltage magnitude
- DC-DC converter efficiency (P_{out} / P_{in})
- Output voltage ripple
- Output load transient response
- Solution complexity
- Switching Frequency (for switch-mode regulators)

Before implementing any design it is important to know which parameters are of the utmost concern. The various concerns could be the optimization for circuit performance, component cost or power density. e.g. if fast transient response or high power density is paramount, then a high operating frequency is in order. On the other hand if high efficiency is the most important parameter to achieve, then a low switching frequency may be the best choice.

The first step in designing the Buck Converter is to determine the values of the inductor and the capacitor in the Output Filter. Based on equations in Chapter 4 (Eq. 4-24) we can make the preliminary calculation.

The specifications for which the Buck Converter has to be designed are as follows:

Input Voltage	1.55 V
Output Power (resistive load)	200 mW
Output Voltage (static requirement)	1V
Allowed Voltage percentage ripple	1%
Allowed current ripple (p-p, ideal source)	20 mA
Minimum efficiency (across voltage, load)	70%

Table 3: Buck Converter Specifications

The applications for which these specifications could be useful for mobile phones (amongst other applications) where there is a continuous demand for progressively lower-voltage supplies.

5.1 Design Equations

The power rating for the load to be driven is 200 mW. So according to this rating the value of load resistance should be 5 Ω. To ensure reliable operation,

inductor must at least be 20% greater than its minimum value and the voltage ripple should be within 1%.

5.2 Input Parameters

For f_{sw} = 100 KHz, ESR = DCR = 1. The reason for selecting these values was because for these values the specifications which are mentioned in Table 3 were met. Using the MATLAB code in Appendix D (which is based around the Type III Compensation mentioned in section 4.8.3), we calculate the values of the different components as mentioned in the section here afterwards.

5.3 Buck Converter Circuit

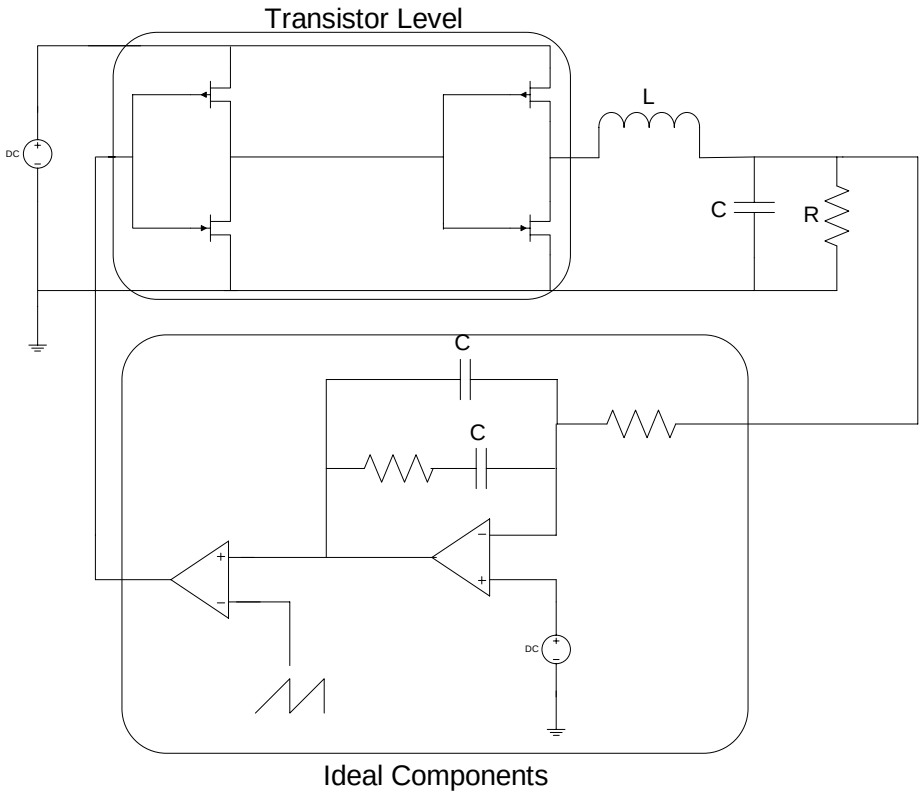

Figure 41: Buck Converter Circuit

Transistors T1 & T2 are sized as 12µ & 6µ respectively and form the driver. T3 is the power switch sized at 1200µ and the low side NFET is 600µ. The large sizing of the transistor has been optimized so as to reduce the resistance and hence the power lost in the switching.

5.4 Calculating Parameters

The values of the capacitor and inductor will vary as can be seen from Eq. 4-25. Different values of the factor LC are included in Appendix A.

The values that have been calculated are for an ideal case, but they do provide us some rough values to start the designing and analysis of our Buck Converter.

C	5 µF
L	88.71µH
R_1	60 kΩ
R_{z2}	153 kΩ
C_{z2}	274 pF
C_{p1}	36 pF
R_{z3}	10 kΩ
C_{z3}	297 pF

Table 4: Calculated Parameters

Based upon these calculated values the corresponding Open Loop Bode Plot's are plotted to ensure that stability will be maintained or not.

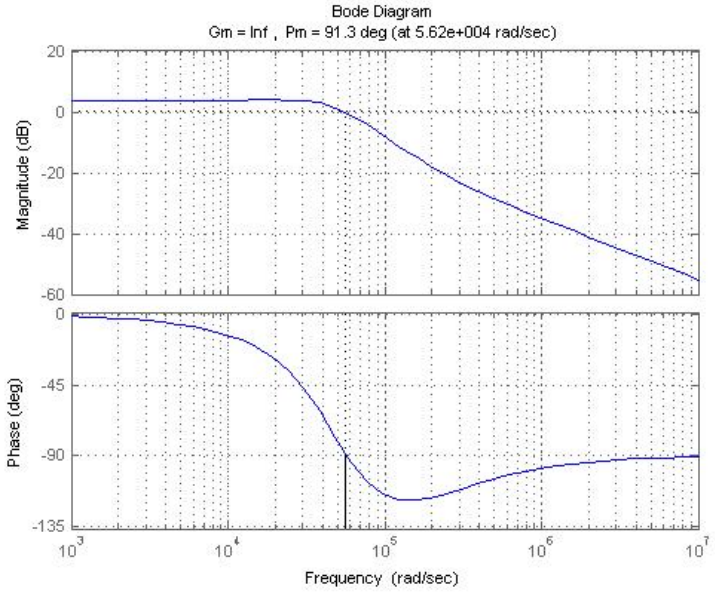

Figure 42: Bode Plot of Buck Converter

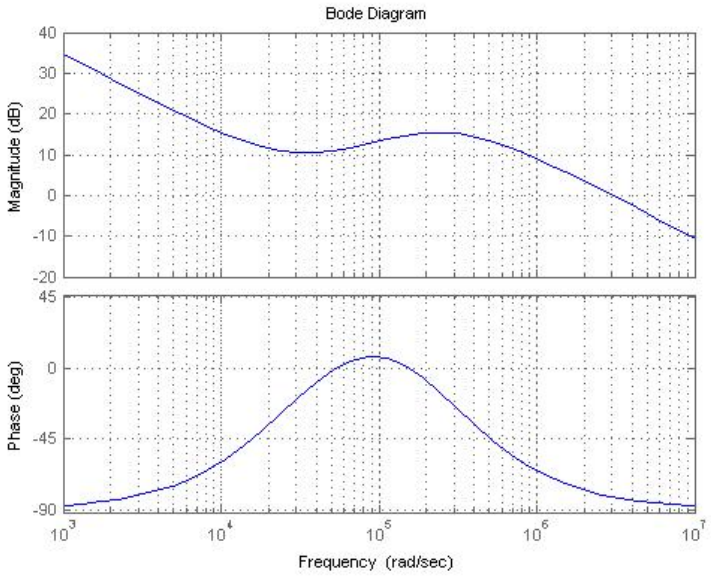

Figure 43: Bode Plot of Type III Compensation Network

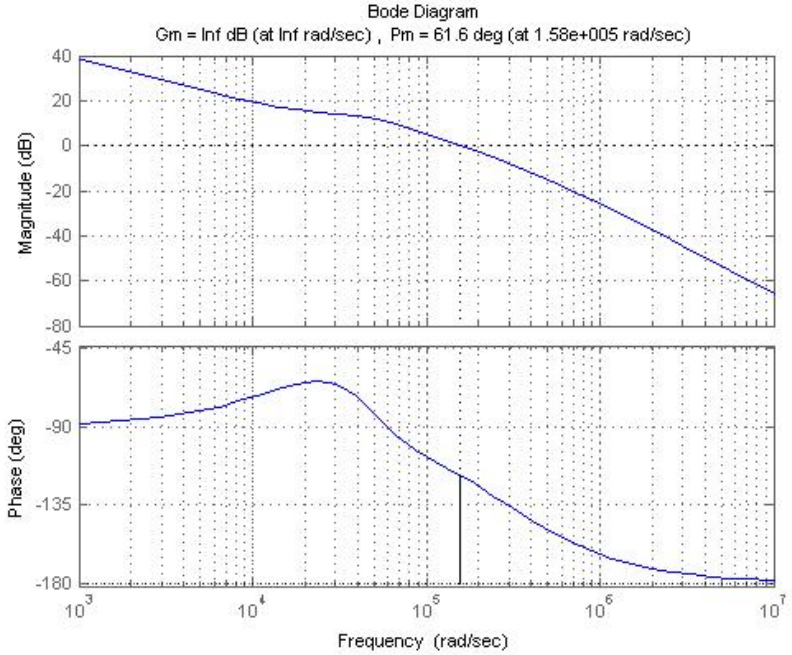

Figure 44: Bode Plot of Total Open Loop Buck Converter

It can been seen from the Figure 43 that the Phase Margin after adding the Type III Compensation is still 61.6° which is good enough to ensure stability. After

confirming this, values are simulated in Cadence which provides us with the following result:

Output Voltage Ripple	12.02 mV
Output Current Ripple	15.1614 mA
Settling Time	329 µs
Average Voltage (Steady State)	995 mV
Power Efficiency	67.9%

Table 5: Results

C	**10 µ**	**5 µ**	**1 µ**
L	44.35 µH	88.7 µH	443.55 µH
R_{z2}	153kΩ	153 kΩ	153 kΩ
C_{z2}	274.1pF	274.1 pF	274.1 pF
C_{p1}	85.33 pF	36.92 pF	6.6657 pF
R_{z3}	10.683 kΩ	10.683 kΩ	10.683 kΩ
C_{z3}	297.96 pF	297.96 pF	297.96 pF
T_s	339.5 µs	459.571 µs	600 µs
V_{ripple}	25.795 mV	13.22 mV	4.1378 mV
I_{ripple}	29.6345 mA	14.8399 mA	2.91053 mA
Output Current	197.6 mA	198.8 mA	199.5 mA
Input Current	187.1 mA	188.3 mA	189 mA
Avg. Voltage	993.9 mV	995.7 mV	998.1 mV
Efficiency	67.7	67.8	67.9

Table 6: For R_L = 5Ω, ESR = DCR = 1, R_1 = 60 kΩ

C	**10µ**	**5µ**	**1µ**
L	44.35 µH	88.7 µH	443.55 µH
R_{z2}	153 kΩ	153 kΩ	153 kΩ
C_{z2}	274.1 pF	274.1 pF	274.1 pF
C_{p1}	85.33 pF	36.92 pF	6.6657 pF
R_{z3}	10.683 kΩ	10.683 kΩ	10.683 kΩ
C_{z3}	297.96 pF	297.96 pF	297.96 pF
T_s	289.7 µs	299 µs	391.63 µs
V_{ripple}	65.97 mV	33.958 mV	13.0125 mV
I_{ripple}	68.033 mA	34.631 mA	7.2641 mA
Output Current	53.47 mA	53.73 mA	52.51 mA
Input Current	45.87 mA	45.44 mA	44.2 mA
Avg Voltage	996.5 mV	1000 mV	999.7 mV
Efficiency (%)	74.9	76.2	76.6

Table 7: R_L = 19Ω, ESR = DCR = 1, R_1 = 60kΩ

	R_L = 5 kΩ	R_L = 19 kΩ
C	5 µF	5 µF
L	88.7 µH	88.7 µH
R_{z2}	153.6 kΩ	153.6 kΩ
C_{z2}	274.1 pF	274.1
C_{p1}	979 fF	979 fF
R_{z3}	10.683 kΩ	10.683 kΩ
C_{z3}	297.96 pF	297.96 pF
T_s	483.71 µs	411.507 µs
V_{ripple}	3.9373 mV	10.62 mV
I_{ripple}	14.81 mA	33.81 mA
Output Current	195 mA	44.63 mA
Input Current	189.8 mA	39.86 mA
Avg. Voltage	998 mV	999.7 mV
Efficiency (%)	66.1	72.21

Table 8: ESR=30E-3, DCR=1, R_1 =60kΩ

From Table 8 it can be seen that with an increase in the R_L the voltage ripple has increased but the efficiency has increased as well.

5.5 Evaluation

5.5.1 Maximum Load

The maximum load that can be driven with the mode still being continuous is **19Ω**. Under this condition the following results arise:

Output Voltage Ripple	36.1538 mV
Output Current Ripple	35.0889 mA
Settling Time	349 µs
Average Voltage (Steady State)	1.0006 V
Power Efficiency	76.1%

Table 9: Maximum Load Conditions

5.5.2 Load Switching

As mentioned earlier through simulations it has been found that the converter stays in the continuous mode for a load that is up to 19Ω. The output in Figure 45 shows the switching. At 450µs the load is switched to 19Ω and at 900µs the load is switched back to 5Ω. For a load of 5Ω the ripple is approximately 1% and increases to about 3% at 19Ω. It is feasible since a maximum of 5% ripple is still tolerable.

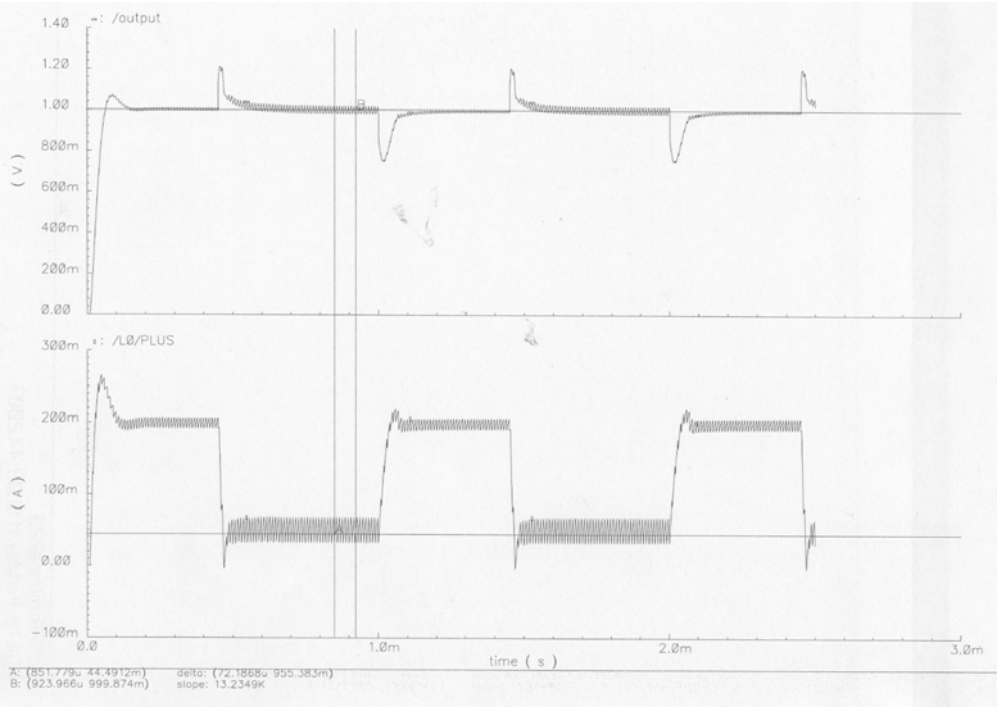

Figure 45: Load Switching from 5Ω to 19Ω

Load Switching was also tested with varying the values of the capacitor and inductor but keeping the switching frequency, ESR & DCR constant. If the capacitor size was increased it resulted in very slow response and if the capacitor size was decreased than overshoots exceeded above 2 V.

5.5.3 Power Efficiency

Power Efficiency of a Buck Converter changes with a change in the load. Efficiency of a Buck Converter is affected by resistive impedances and the switching losses due to the capacitive parasitic impedances of the circuit components [9].

$$Efficiency = \frac{OutputPower}{InputPower} = \frac{OutputVoltage \times OutputCurrent}{InputVoltage \times InputCurrent}$$

5.5.4 Chip Area

According to the values stated in Table 4 the following is the area approximation in 90nm library.

5.5.4.1 Capacitor

cmimmk

Width (µm)	Length (µm)	Area (µm)^2	Value (F)
16.5	9060.5	149498.2	299.9 p
15	1200	18000	36.11 p
15.5	9000.5	139507.8	279.9 p

cpo25w

Width (µm)	Length (µm)	Area (µm)^2	Value (F)
16	3200	51200	297.5 p
16	390	6240	36.27 p
16	2950	47200	274.3 p

5.5.4.2 Resistor

rnwod (N-well Resistor)

Width (µm)	Length (µm)	Area (µm)^2	Value (Ω)
5	2200	11000	154 k
1.8	55	99	10.69 k

rpporpo (Unsilicided P+ PolyRes)

Width (µm)	Length (µm)	Area (µm)^2	Value (Ω)
1	22	22	10.538 k
1	320	320	152.136 k

rhiporpo (High Resistance Poly Res)

Width (µm)	Length (µm)	Area (µm)^2	Value (Ω)
1	10	10	10.463 k
1	145	145	154.233 k

5.9 Conclusion

This thesis work has given a basic insight in to the working of a buck converter that could be considered to be manufactured on-chip. Though a few of the issues have not been solved but they have been highlighted as potential areas in which more refinements are required. The affect of the system when R_L switches from one value to another have also been observed. Though we have considered the ideal cases only but if all non-ideality would be considered than we would see that ripple would increase and the efficiency would also decrease.

5.10 Future Work

Most of the simulations have been done using ideal components or modelled in Verilog A code. It would be a good challenge to include the transistor level modelling there and see the responses of the overall system. Eventually the layout for a fully testable and working DC-DC Converter could be done in 90nm process. Extensive study was not made into the reduction of the overshoot that is observed in the output in Figure 45 and main emphasis remained on the ripple during steady state.

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Appendix

Appendix A – Values of L&C

Using Eq. 4-25 we can calculate the factor of LC for a particular switching frequency and allowed ripple. This LC factor can be adjusted with the value of the Capacitor and the Inductor that we desire.

V_{in} = 1.2V & V_{out} = 1V
For 1 % Ripple, the following formula (derived from Eq. 4-25) can be used:

$$LC = \frac{(1/f_{sw})^2(0.1667)}{8 \times 0.01}$$

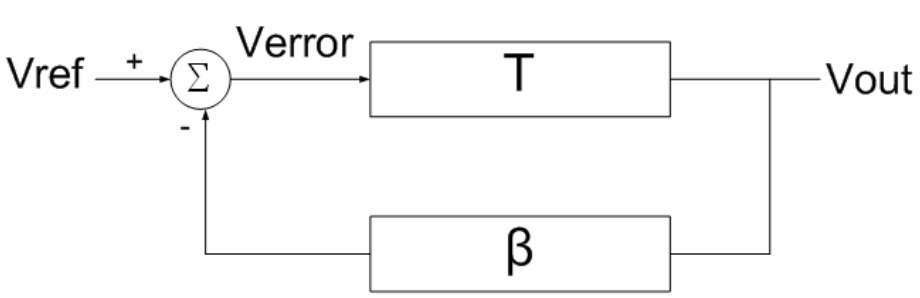
For 5 % Ripple, the following formula (derived from Eq. 4-25) can be used:

$$LC = \frac{(1/f_{sw})^2(0.1667)}{8 \times 0.05}$$

f_{sw}	**100 kHz**		**200 kHz**		**300 kHz**	
ΔV	1%	5%	1%	5%	1%	5%
LC	20E-12	41.7E-12	52E-12	10.5E-12	23E-12	4.63E-12

f_{sw}	**400 kHz**		**500 kHz**		**1 MHz**	
ΔV	1%	5%	1%	5%	1%	5%
LC	13E-12	2.6E-12	8.3E-12	1.6E-12	2.08E-12	0.42E-12

Appendix B - Open Loop & Closed Loop



Appendix Figure 1: Feedback Loop

The open-loop system gain or *open-loop transfer function* is T. Solving for V_{out} results in the *closed-loop transfer function*

$$[V_{out} - V_{out}\beta]T = V_{out}$$

Solving for V_{out}, the result is the *closed-loop transfer function*

$$V_{out} = \frac{T}{1+\beta T} \cdot V_{ref}$$

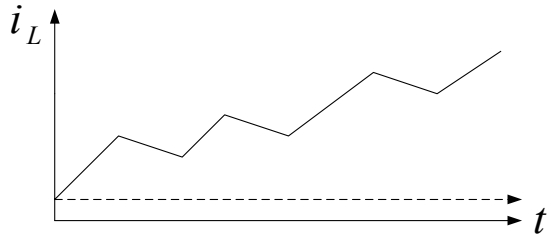
The symbol K can be used for this function, so that $V_{out} = K \cdot V_{ref}$. The error function $v_{error} = V_{ref} - V_{out} \cdot \beta$ is given by

$$v_{error} = \frac{1}{1+\beta T} V_{ref}$$

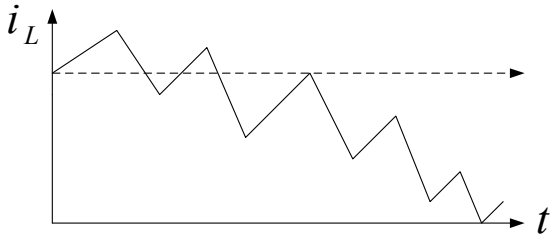
Notice that the error can be made small with a large value for H(s). This is exactly the principle of high-gain feedback. It is convenient to move the feedback loop gain β through the summing block as in Appendix Figure 1 to form an *equivalent open-circuit transfer function, βT.* This function represents the signal to be subtracted as feedback, and is very useful for stability analysis. The equivalent feedback is unity in this case.

If the open-loop and feedback loop gains β & T are positive, the open-loop gain is always higher than the closed loop gain. The effect is that more *control energy* will be necessary for a closed loop system than for the open-loop case. In many systems – particularly power converters – there are physical limits on the input signals. Thus physical limitations and stability constraints limit the practical value of β.

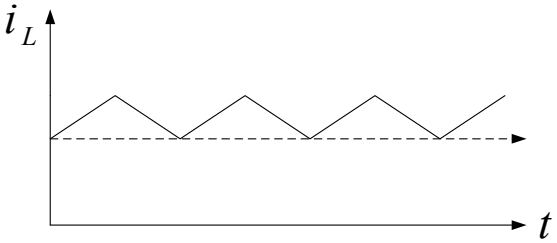
Appendix C - Steady-State Operation



Appendix Figure 2: Unstable Current



Appendix Figure 3: Decaying Current



Appendix Figure 4: Steady-State Current

Steady-state operation requires that i_L at the end of switching cycle is the same at the beginning of the next cycle. That is the change of i_L over one period is zero, i.e.:

$$(\Delta i_L)_{closed} + (\Delta i_L)_{opened} = 0$$

$$\left(\frac{V_d - V_o}{L}\right) \bullet DT_s - \left(\frac{-V_o}{L}\right) \bullet (1-D)T_s = 0$$

$$\Rightarrow V_o = DV_d$$

Appendix D – MATLAB Code

```
% Calculates all the values and plots all the graphs for a Type III
% Compensation

Vd = 1.55
Vo = 1
Vr = 1
R = 5

fsw = input('Enter Switching Frequency in KHz ');
Ripple = input('Enter allowed % ripple ');
fsw = fsw*1E3
deltaV = (Ripple/100)*Vo
DC = Vo/Vd;
LC = 0.125*((1/fsw)^2)*(1-DC)*(Vo/deltaV)

C = input('Enter value of C in uF ');
C = C*1E-6;
L = LC/C

R1 = input ('Enter value of R1 (K) between 2 & 5 ');
R1 = R1*1E3;
rC = input ('Enter value of ESR ');
rL = input ('Enter value of DCR ');
DBW = 0.3*fsw

FESR = 1/(2*3.1415926535*rC*C)
FLC= 1/(2*3.1415926535*sqrt(L*C))
Rz2 = (DBW/FLC)*(Vr/Vd)*R1
Cz2 = 1/(3.14159*Rz2*FLC)
Cp1 = Cz2/((2*3.14159*Rz2*Cz2*FESR)-1)
Rz3 = R1/((fsw/(2*FLC))-1)
Cz3 = 1/(3.14159*Rz3*fsw)

s = tf('s');

% Transfer Function of Buck Converter
G = Vd/Vr;   % 1/Vr is the effect of the PWM
N = 1+s*(rC*C);
D = 1+s*((L+((rC+rL)*R*C))/R)+(s^2)*(L*C);

Buck = (G*(N/D));
figure(1)
margin(Buck)
grid
```

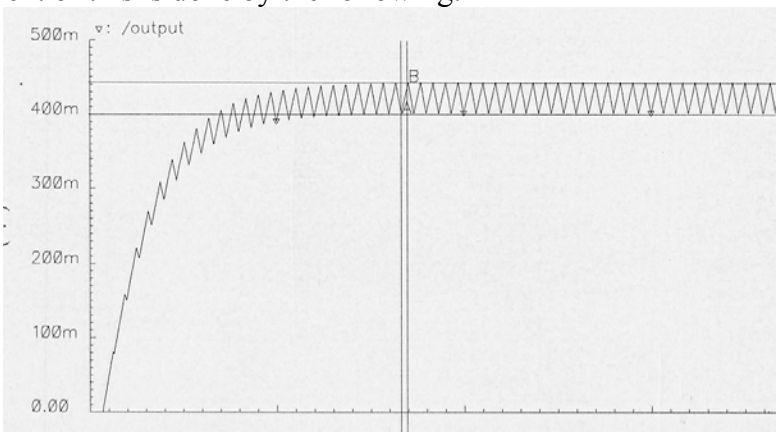
```
G1 = (R1+Rz3)/(R1*Rz3*Cp1);
N1 = s + (1/(Rz2*Cz2));
N2 = s + (1/((R1+Rz3)*Cz3));


D0 = s;
D1 = s + ((Cp1+Cz2)/(Rz2*Cp1*Cz2));
D2 = s + (1/(Rz3*Cz3));


Type3 = G1*((N1*N2)/(D0*D1*D2));
figure(2)
bode(Type3)
grid

BuckType3 = Buck*Type3
figure(3)
margin(BuckType3)
grid
L, C, rC, rL, R1, Rz2, Cz2, Cp1, Rz3, Cz3, fsw
```

Measurement of this is done by the following:



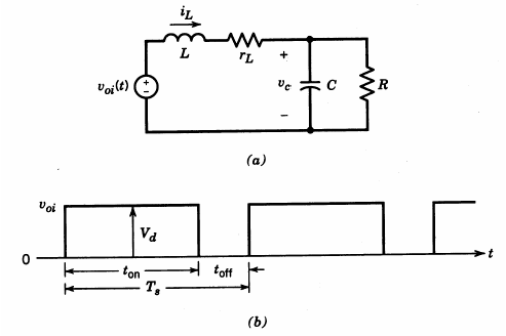
Appendix Figure 5: Measuring Ripple

The ΔV is calculated by adjusting the A crossbar first on the point on which the lower side ripple do not fall beyond it. The same applies for B. Where these two conditions are met we calculate the value and assume that the circuit is now in steady state.

Appendix F - Linear Differential Equations

The Appendix Figure 6 shows a simplified equivalent circuit to represent a switch-mode, regulated voltage supply. The same circuit topology applies in both states of the switch. The only difference is that $v_{oi} = V_d$ when the switch is on, otherwise $v_{oi} = 0$. The inductor resistance r_L is included.

The waveform of the voltage v_{oi} is shown in Appendix Figure 6, where the switch duty ratio $D = t_{on}/T_s$ is dictated by the controller in the actual system, based on operating conditions.



Appendix Figure 6: Buck Converter [1]

The equations are written in terms of the capacitor voltage v_c and the inductor current i_L, the so-called state variables, since they describe the state of the circuit. It is assumed that at time t=0 at the beginning of the simulation, the inductor current $i_L(0)$ and the initial capacitor voltage $v_c(0)$ are known. By applying Kirchoff's current law (KCL) and Kirchoff's Voltage Law (KVL) in the circuit of Appendix Figure 6b, we get the following two equations:

$$r_L i_L + L\frac{di_L}{dt} + v_c = v_{oi} \qquad \text{(KVL)}$$

$$i_L - C\frac{dv_c}{dt} - \frac{v_c}{R} = 0 \qquad \text{(KCL)}$$

By dividing both sides of Eq. by L and Eq. 2 by C, we can express them in the usual state variable matrix form

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{oi}(t)$$

The above equation can be written as

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}\mathbf{x}(t) + \mathbf{b}g(t)$$

Where **x**(t) is a state variable and g(t) is the single input:

$$\mathbf{x}(t) = \begin{bmatrix} i_L \\ v_c \end{bmatrix} \text{ and } g(t) = v_{oi}$$

The matrix **A** and the vector **b** are

$$\mathbf{A} = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \text{ and } \mathbf{b} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

Appendix G - Development Work Flow